

# International collaboration - **Joint call** **EU and Japan on semiconductors**

Topic: DIGITAL-JU-Chips-2026-SG-JAPAN

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# EU-Japan Call on semiconductors

[Text is tentative and subject to change!]

- Type of Action                      Single Grant (Digital Europe Programme)
- Indicative Budget                      Euro 5-15 million
- Expected EU contribution per project                      Euro 5 million
- Mode                      co-funded with NFA,  
one stage call
- Technology Readiness Level (TRL)                      from <5 to 7
- Call launch date                      07 July 2026
- Deadline                      17 September 2026

# EU-Japan Call on semiconductors

## Context

- Advancing AI-enabled technologies and scaling chip architectures to node sizes below 2nm
- Balance performance and power efficiency
- Improve materials, equipment and process technologies

## Focus

- Fostering a robust chiplet ecosystem to enable heterogeneous integration for the AI stack
- Advancing process technologies for next-generation, cutting-edge nodes

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## Participation

- EU entities
- Japanese entities with domestic funding

## Mode of cooperation envisaged

- Two frameworks/contracts per project (EU and JPN)
- Cross-referencing of workpackages and partners

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## Expected Outcomes

- Advanced heterogeneous integration, particularly in 2.5D and 3D packaging, to support AI functionalities.
- Standardised chiplet interfaces, enabling interoperability and fostering a dynamic chiplet ecosystem.
- Process technologies for device structures beyond 2nm, such as CFET, enabling high-performance and energy-efficient solutions that meet next-generation demands.
- Contributions to international standard setting for chiplet integration.

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## Scope

- Develop methods for chiplet co-optimization, interface design, and 2.5D/3D integration processes, including through-silicon vias, interposers, and bonding techniques.
- R&I on advanced fabrication processes such as thin film deposition, etching, and doping for devices that incorporate CFET or vertically stacked GAA switches, to enhance performance and reduce power consumption.

## Addressed stakeholders

- Engage material scientists, chemical engineers, semiconductor manufacturers, and AI experts to bridge research and industrial applications, supporting broad adoption and commercial viability