Chips JU Calls 2026
Chips for Europe Initiative

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EUROPEAN
PARTNERSHIP

Chips for Europe Initiative

- HE Actions

Description	Indicative EU budget M€
Quantum Chips Design: Driving Europe's Quantum Design Ecosystem and Enabling Quantum Design Tools Innovation	**30**
Quantum Chips: Enabling Technologies	**20**
Total	**50**

Chips for Europe Initiative

- DEP Actions

Description	Indicative EU budget M€
Call for Design Enablement Teams	**5**
Skills Hubs of Excellence	**20**
Pilot Federation	**10**
Stimulation of Chip Design	**15**
International collaboration - Joint call EU and Japan on semiconductors	**15**
AI chips and systems for EU compute infrastructure	**100**
Total	**165**

Skills: Pilot Federation

- Projects funded under this call establishing the ‘Pilot Federation’ should network European VET providers with focus on vocational training.
- Projects should deliver several of the following elements:
  - Provide a **comprehensive overview of the micro-credential offer** and the **relevant providers** in the semiconductor sector in Europe.
  - Develop a **pilot scalable network of VET providers** and an industry-aligned micro-credentials ecosystem in Europe for the semiconductor sector.
  - Design **training programmes through partnerships among VET providers** and business to **align courses more closely with industry needs** with **focus on reskilling** programmes for professionals transitioning from other industrial sectors experiencing surplus workforce.
  - Place **emphasis on micro-credentials**, a flexible tool for rapid upskilling and lifelong learning.
  - **Encourage cross-border collaboration**.
  - **Attract extra-EU migration** of workers

Skills: Pilot Federation

Type of Action	Simple Grant
Indicative EU budget	**10 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of around EUR **10 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call with submission of Full Proposal (FPP)
Call launch date	*07 Jul 2026*
Deadline FPP Phase	*17 Sep 2026 at 17:00 Brussels Time*

Skills: Stimulation of Chip Design

- **Organising and implementing a comprehensive Chip Design Skills Programme** aimed at inspiring new generations to pursue careers in the semiconductor sector.
- **For students at both higher education** institutions in relevant disciplines **and secondary schools**.
- To be **developed as part of a broader continuum of European semiconductor skills initiatives**, ensuring strong complementarities and synergies with existing efforts such as **EUROPRACTICE** and the **Design Platform** and **Competence Centres**.
- Activities should be **widely disseminated** and **accessible** to relevant parties **in all EU 27 Member States**.

Skills: Stimulation of Chip Design

Type of Action	Coordination and Support Action (**CSA**)
Indicative EU budget	**15 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of around **EUR 15 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	EU funding only One stage Call with submission of Full Proposal (FPP)]
Call launch date	*07 Jul 2026*
Deadline FPP Phase	*17 Sep 2026 at 17:00 Brussels Time*

Skills Hubs of Excellence

- Proposals submitted under this topic establishing a ‘Hub of Excellence’ should support high education topics for skills development **to address talent shortages** in targeted fields: **chips design**, **chips manufacturing**, **advanced packaging** and **testing**, **photonics**.
- Projects should include several of the following elements:
  - Design **educational programmes through partnerships among universities and business** to align academic programmes more closely with industry needs.
  - **Projects should** host and **support**, together with industry co-funding, educational infrastructures for students’ **access to modern processing equipment**.
  - Programmes **should promote STEM and diversity inclusion**.
  - **Ease intra-EU mobility of students** from countries with an historical surplus of graduates in semiconductor related studies.
  - **Encourage cross-border collaboration** while tailoring education to specific regional and national needs.
  - **Attract extra-EU migration** of students.
  - **Establish accessible career-orientation platforms** and public awareness campaigns across European countries.

Skills Hubs of Excellence

The text in this subsection should be seen as a placeholder.
The exact manner in which the funding will be allocated will be defined in a later stage.

Type of Action	Simple Grant
Indicative EU budget	**20 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of around EUR **10 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call with submission of Full Proposal (FPP)
Call launch date	*07 Jul 2026*
Deadline FPP Phase	*17 Sep 2026 at 17:00 Brussels Time*

Quantum Chips Design: Driving Europe's Quantum Design Ecosystem and Enabling Quantum Design Tools Innovation

- **Foster a pan-European community around quantum chip design**.
- **Research, development, and validation of European quantum design tools**, covering chip design, layout, simulation, verification, and flow integration, including Process Design Kit (PDK) interface coding, software layers, APIs, and data.
- **Effective progression from community alignment to operational deployment**
- **Establishing formal interfaces and operating procedures with relevant Chips JU pilot lines** (including quantum-focused Quantum Pilots) and European pilot lines in microelectronics and photonics.
- The action should **ensure interoperability across platforms**, reduce duplication of effort, and **establish a sustainable repository of fully verified and validated design libraries**.
- **Connect design with fabrication**, to support quantum-compatible fabrication access.
- Proposals should document **concrete access arrangements to at least one relevant pilot line/foundry** and demonstrate **alignment with the European Design Platform** onboarding process.

Quantum Chips Design: Driving Europe's Quantum Design Ecosystem and Enabling Quantum Design Tools Innovation

Type of Action	Research and Innovation Action (**RIA**)
Indicative EU budget	**30 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of around **EUR 30 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call with submission of Full Proposal (FPP)
Call launch date	*07 Jul 2026*
Deadline FPP Phase	*17 Sep 2026 at 17:00 Brussels Time*

Quantum Chips: Enabling Technologies

- This topic focuses on enabling technologies that support, control, and read out quantum systems without funding the core quantum chips themselves
- Proposals should target **system-level integration and interfaces**. Solutions may include for example:
  - **Control and readout electronics** across temperature stages including cryogenic
  - **Photonic/optical components** for routing, modulation, detection and timing
  - **Transduction and networking technologies** such as microwave-optical conversion
  - **Cryogenics, interconnects, packaging and heterogeneous integration** for modular assemblies
- The topic **covers two complementary categories of enabling technologies**:
  - Process Enabling Technologies
  - Operations Enabling Technologies.
- This topic **does not fund the manufacturing of core quantum chips/QPUs**.

Quantum Chips: Enabling Technologies

Type of Action	Research and Innovation Action (**RIA**)
Indicative EU budget	**20 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of around **EUR 5 to 7 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	**Co-funded with the NFA** One stage Call with submission of Full Proposal (FPP)
Call launch date	*07 Jul 2026*
Deadline FPP Phase	*17 Sep 2026 at 17:00 Brussels Time*

International collaboration - Joint call EU and Japan on Semiconductors

- The scope includes, but is not limited to, the following areas:
  - Develop **methods for chiplet co-optimization**, **interface design**, and **2.5D/3D integration** processes, including through-silicon vias, interposers, and bonding techniques.
  - **R&I on advanced fabrication processes**.
  - Engage material scientists, chemical engineers, semiconductor manufacturers, and AI experts to bridge research and industrial applications, supporting broad adoption and commercial viability.

Proposals should **encourage partnerships across industry, academia, and research organizations** to foster breakthroughs in semiconductor manufacturing and contribute to advancing global semiconductor standards.

International collaboration - Joint call EU and Japan on Semiconductors

The text in this subsection should be seen as a placeholder.
The exact manner in which the funding will be allocated will be defined in a later stage.

Type of Action	Simple Grant (**SG**)
Indicative EU budget	**15 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of around **EUR 5 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	**Co-funded with the NFA** One stage Call with submission of Full Proposal (FPP)
Call launch date	*07 Jul 2026*
Deadline FPP Stage	*17 Sep 2026 at 17:00 Brussels Time*

Call for Design Enablement Teams

- Each **DET is in charge managing a distributed cloud instance** and **providing dedicated application engineering support** to users from setting up their design environment and design flows up to tape-out.
- A **DET can be a single entity**, **or a consortium** of entities selected among providers of chips design support services, such as design houses, RTOs or other entities currently providing design enablement services on a commercial basis.
- **DETs should be selected based on their technology expertise**, ability to offer support across the end-to-end design flow, **access to fabrication services** (foundries, packaging, test services) and a **proven track record** of delivering high quality services to users, amongst other characteristics.

Call for Design Enablement Teams

The text in this subsection should be seen as a placeholder.
The need for additional DET will be defined in a later stage.

Type of Action	Coordination and Support Action (CSA)
Indicative EU budget	**5 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of around **EUR 0.5 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	**EU funding only** One stage Call with submission of Full Proposal (FPP)
Call launch date	*07 Jul 2026*
Deadline FPP Phase	*17 Sep 2026 at 17:00 Brussels Time*

AI chips and systems for EU compute infrastructure

- Proposals submitted to this call are expected to address the following elements:
  - The consortium will form a buyers' group of procurers under EU law, that will set up and run a Pre-Commercial Procurement (PCP) in staged phases, ensuring competition to the end.

AI chips and systems for EU compute infrastructure

The text in this subsection should be seen as a placeholder.
The exact manner in which the funding will be allocated will be defined in a later stage.

Type of Action	Grant for Procurement
Indicative EU budget	**100 M€**
Expected EU contribution per project	The JU estimates that an EU contribution of **EUR 100 million** would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	**Co-funded with the NFA** One stage Call with submission of Full Proposal (FPP)
Call launch date	*07 Jul 2026*
Deadline FPP Phase	*17 Sep 2026 at 17:00 Brussels Time*

PLANNING CHIPS-JU ECS CALLS 2026