



# Quantum Design & Quantum Enabling Technologies: Introduction to the topics

ECS Brokerage Event, 5 February 2026

*DG CNECT.C2 – Quantum Technologies  
Enabling and Emerging Technologies  
European Commission*

# Outlook

1. The EU Context
2. The EU Chips Act
3. The Quantum Europe Strategy

# 1. The EU Context

1. The EU Context

2. The EU Chips Act

3. The Quantum Europe Strategy

# EU Initiatives building the Quantum Ecosystem

Equity Investments &  
Support to Start-ups

€ 300 M

IRIS<sup>2</sup> (Secure  
Connectivity)  
& EuroQCI

€700 M



**EuroHPC**  
Joint Undertaking

4  
€300 - 400 M

## Quantum Flagship

€1000 M

TECHNICAL PILLARS



Terrestrial,  
airborne and  
space gravimetry

CROSS-CUTTING ACTIVITIES

ENGINEERING /CONTROL  
EDUCATION/TRAINING  
SOFTWARE/THEORY

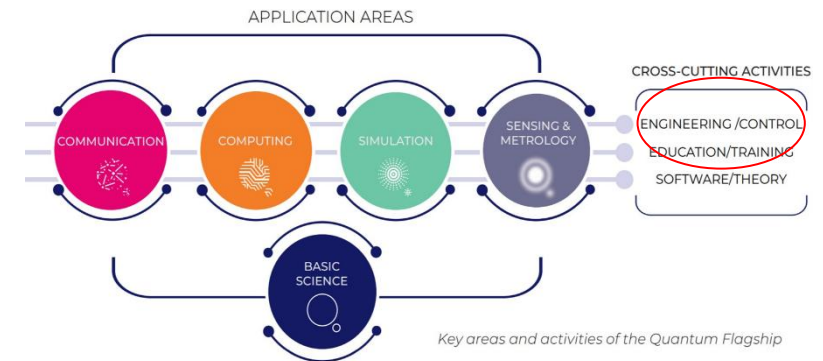
Chips Act €400 M

Skills &  
Education

€25 M

# Quantum Flagship: Fostering Industrial Uptake of QT

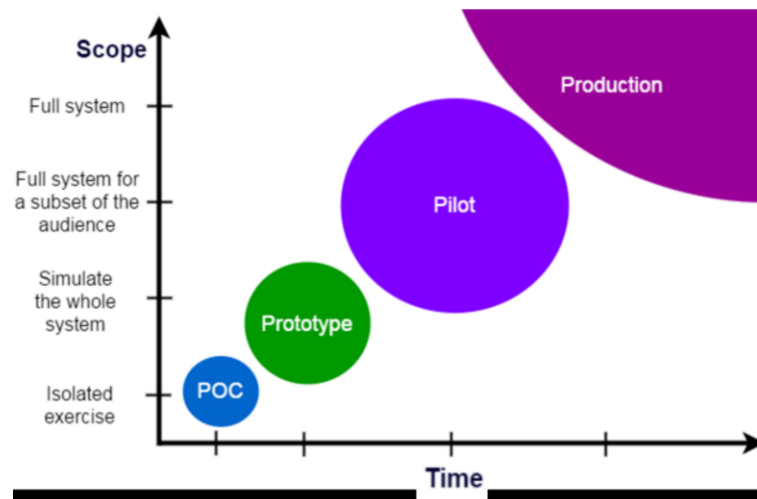
Experimental production and testing capabilities for QT



**QU-PILOT** (FPA/SGA1: 19M€, 10 RTOs, 11 companies)

Start April 2023, End October 2026

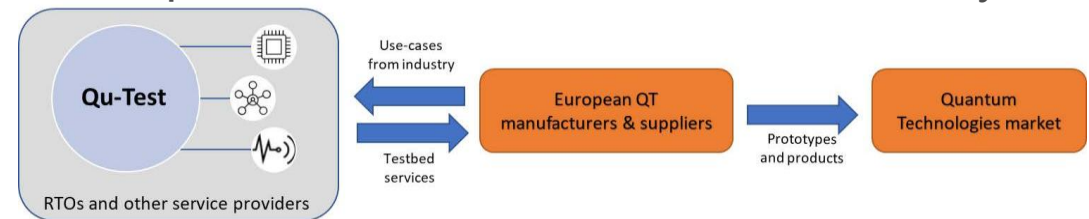
Goal: Establish engineering methods and processes that are scalable at industrial level



**QU-TEST** (FPA/SGA1: 19M€, 13 RTOs, 12 companies)

Start April 2023, End October 2026

Goal: Establish a (open-access) network of QT testing and experimentation infrastructure for industry needs



# 2. The EU Chips Act

1. The EU Context

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# Chips for Europe Initiative

Aim: bridging the gap from lab to fab

## 5 Objectives

- 1 Reinforce design capacity by providing a **virtual design platform**
- 2 Enhance existing and developing new **pilot lines**
- 3 Accelerate the development of **quantum chips**
- 4 Expand **skills** and set up a network of **competence centres**
- 5 Facilitate SME access to **equity and loans** through a dedicated **Chips Fund**

Chips JU

EIC  
I-EU

Basic  
Research

Applied  
Research

Prototyping

Pilot lines

Production



European  
Commission



# High diversity of quantum chips

And diversity and synergies of different quantum pillars →

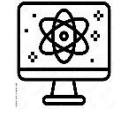
Examples of EU expertise, capability and products



QUANTUM SENSING



QUANTUM COMMUNICATION

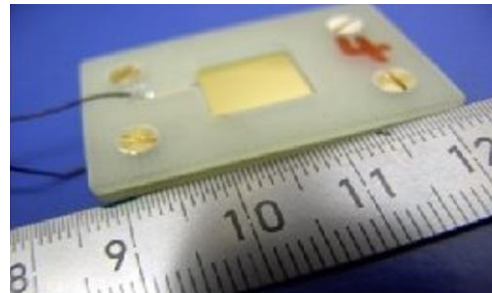


QUANTUM COMPUTING

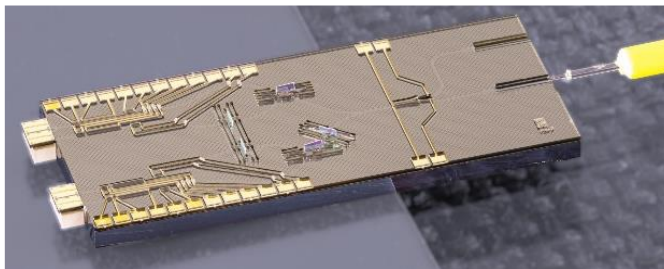
quantum chip technology tailored to meet the specific qubit requirements for computing, sensing, and communication, ensuring optimal performance for each application.



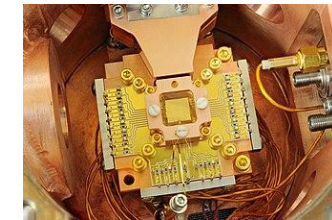
Computing: **Superconducting qubits** and parametric amplifier (for control and readout of qubits)



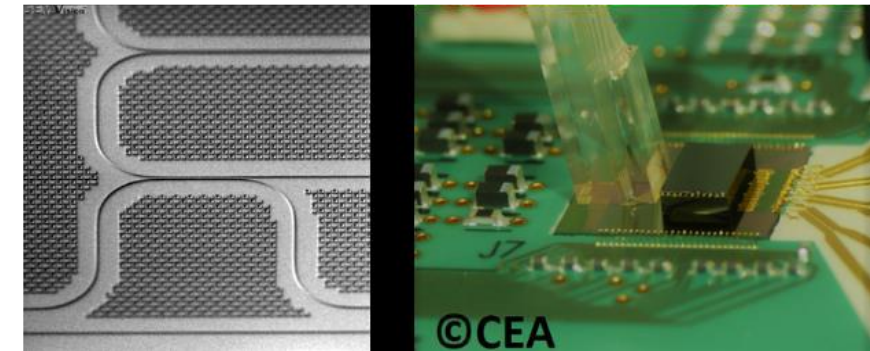
Sensing/Communication/Computing: Diamond growth, defect implantation (**NV-Center**), characterization



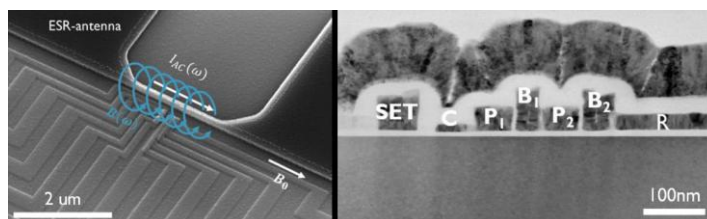
Communication: Polarization coding **BB84 transmitter PIC**



Computing/Sensing: (Left) **Trapped ions Paul trap**, (Right) **Chip ion trap**



Communication/Computing: (Left) SEM view of a **silicon photonic circuit** for entangled photon generation (Right) Packaging of **photonic integrated circuits** with fiber array and electronic chip on top



Computing: **Silicon spin qubit** cell with ESR manipulation unit: top view (left) and cross-section (right)



# Co-creation process

## Phase 1

- With the quantum community, Quantum Flagship SAB & QUIC
  - Provided technical input for roadmap ([SRIA](#))
- Technical Workshops and feedback from Experts

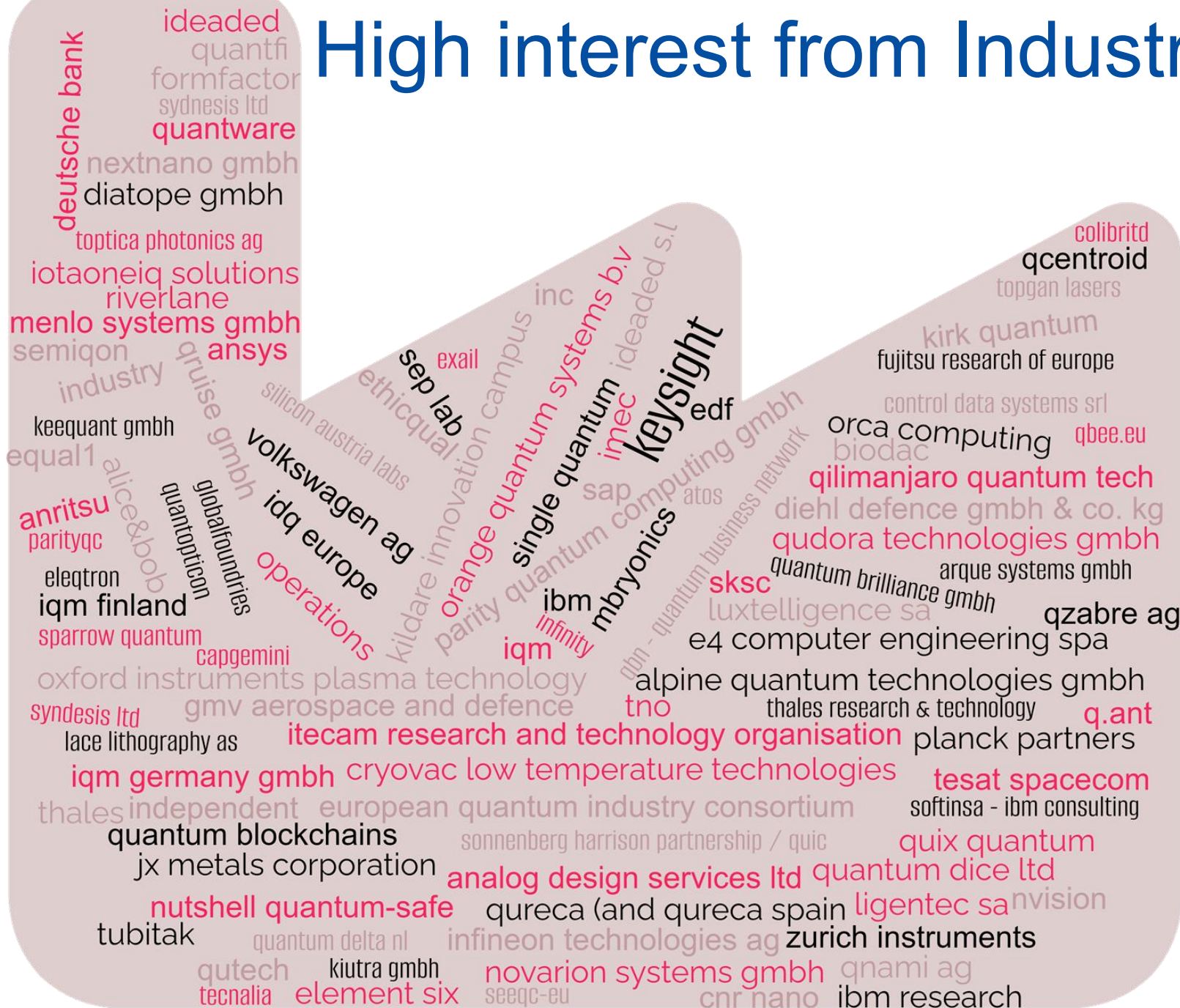
## Phase 2

- With the Member States, National Quantum Initiative representatives
  - Informal group for MS consultation
  - Creation of 6 Interest Groups per technology

## Phase 3

- With the Chips JU, GB chips JU (Concept mature to review with GB)
  - Provide feedback to Roadmap and calls
  - Approval of the Work Programme

# High interest from Industry participants...

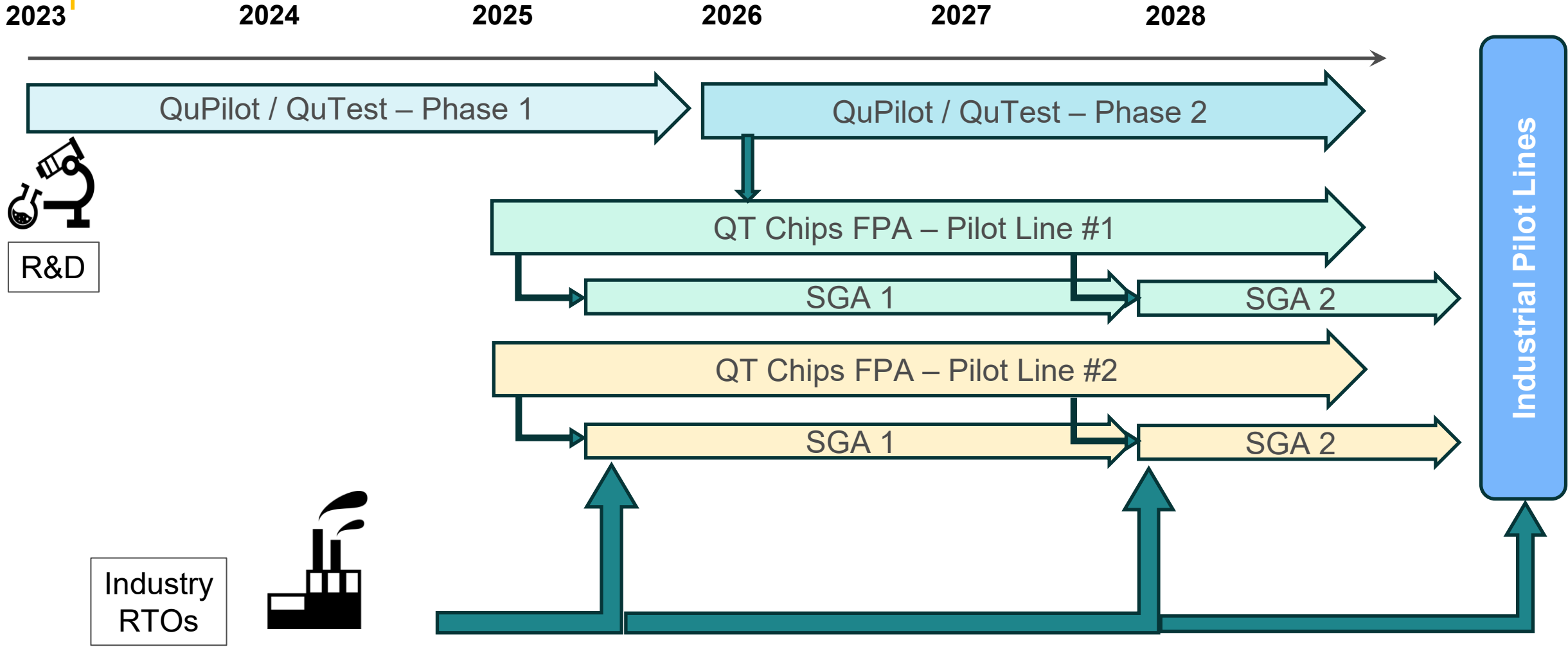


**Globalfoundries**  
**Infineon Technologies AG**  
**IBM Research**  
**Formfactor**  
**Ansys**  
**Anritsu**  
**Keysight**  
**Fujitsu Research of Europe**  
**Silicon Austria Labs**

# Maturity of manufacturing technologies

Technology Platform	Communications	Computing/Simulation	Sensing & Metrology
Superconducting	Cryogenic temperature	Leading in quantum processors and annealers	metrology and magnetic field sensors
Photonics	Room temperature, QKD over long distances	Room temperature, challenges in noise reduction	research for applications like LIDAR
Semiconducting	Potential in integrated quantum circuits	Spin qubits are promising for scalable quantum computers	Used in high-resolution and sensitive detectors
Trapped Ions	Room temperature, main focus on computing	high-fidelity qubits with long coherence times	precision measurements but require complex setups
Diamond	Main focus is on sensing applications	Studied for use as robust qubits	High-precision sensors at the nanoscale
Neutral Atoms	Experimental stage for secure communication	Promising results, challenges in scalability and error correction	Mature applications, e.g. atomic clocks, interferometers

# Overall concept



# The Roadmap to industrialisation

## ...From pilot lines to industrialization

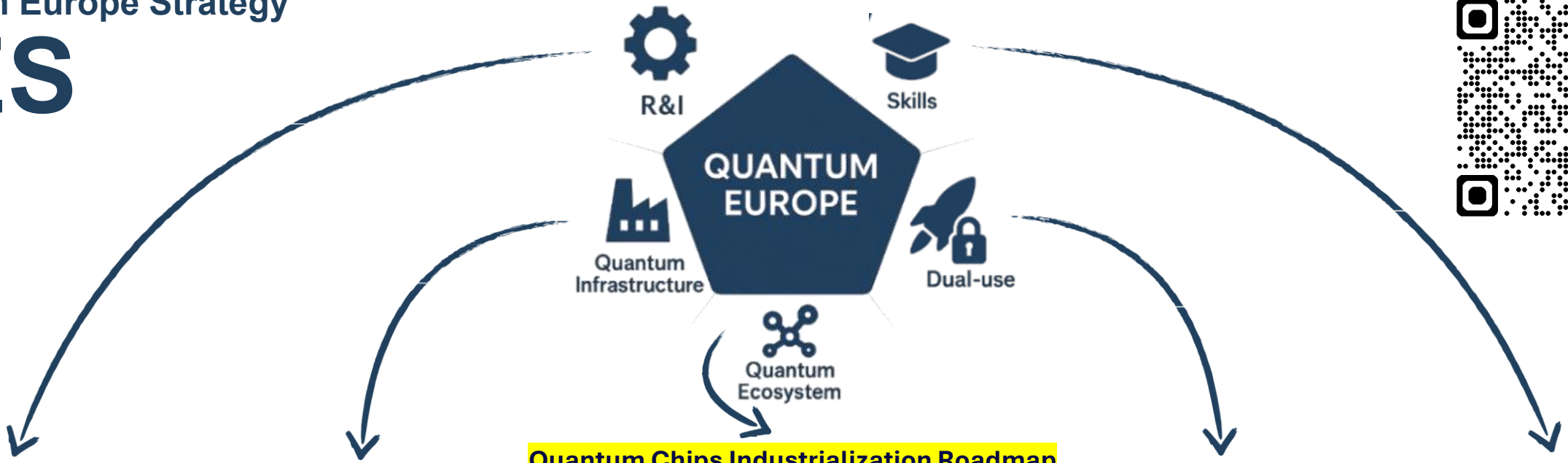
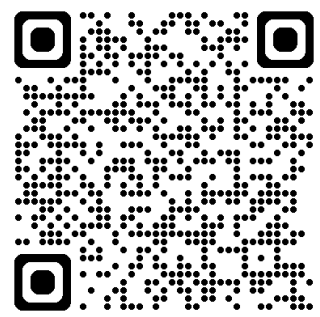
Quantum chips are not standalone products, their industrialization depends:

1. Quantum Enabling Technologies → essential to scale quantum chips
  - a. Cryogenics, control electronics, packaging, interconnects, etc., determine yield, reliability and cost
  - b. How to define them & how to link them with the Quantum Pilot Lines?
2. Quantum Design → required for manufacturable and usable chips
  - a. Systematic architectures and co-design are needed for reproducibility, scalability, etc.
  - b. What are the quantum-specific design tools & how to include them in the European Design Platform?



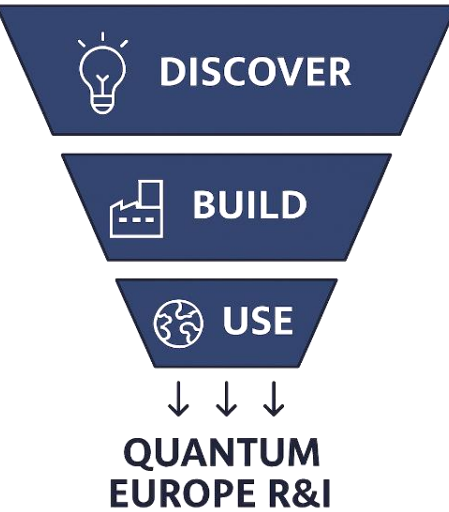
Quantum Europe Strategy

# QES

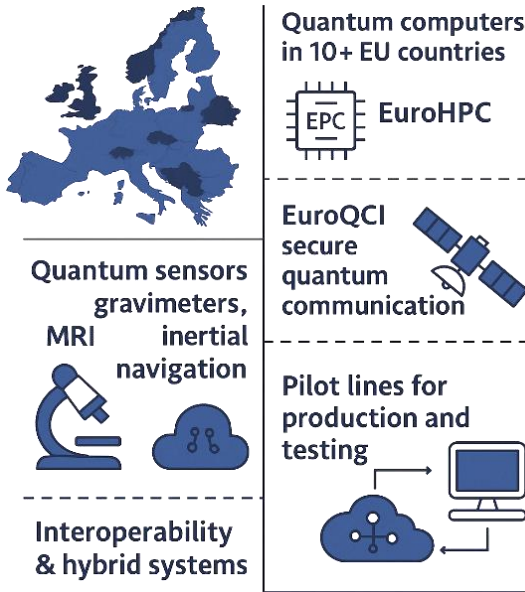


Quantum Chips Industrialization Roadmap

FROM LAB TO MARKET



SCALING QUANTUM CAPABILITIES



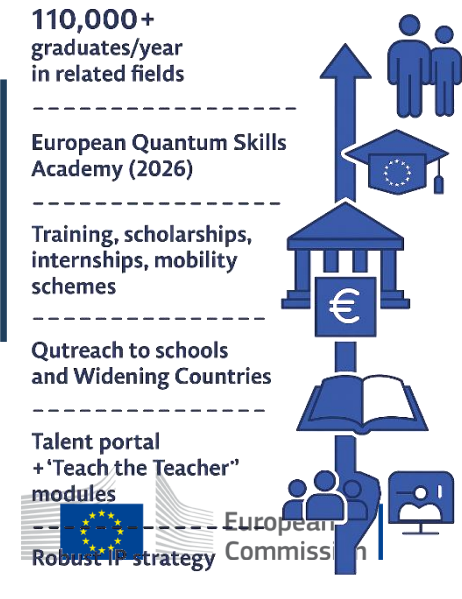
GROWING EUROPE'S QUANTUM ECONOMY



STRATEGIC AUTONOMY IN SPACE, SECURITY & DEFENCE



A QUANTUM WORKFORCE FOR THE FUTURE







# Thank you for your attention



# Calls on Quantum Chips: Enabling Technologies and Design

Cecilia Gonzalez Alvarez – Programme Officer

5<sup>th</sup> February 2026



# Quantum Enabling Technologies topic outline

Refer to Appendix 8 of Work Programme p. 44

[https://www.chips-ju.europa.eu/GB\\_2025.125\\_Appendix8\\_2026\\_CElv1.pdf](https://www.chips-ju.europa.eu/GB_2025.125_Appendix8_2026_CElv1.pdf)

# Expected outcomes – Important dimensions to consider

- Platform-agnostic usability of enabling subsystems **across at least 2 quantum platforms**
- Miniaturisation and subsystem assembling enabling **higher-scale quantum systems**
- **Evidenced** manufacturability and reliability gains
- Strengthened European supply capability and reduced dependency on non-EU sources for critical parts
- Compatibility with microelectronics infrastructure

# Expected outcomes – Common requirements to all proposals

- **No funding to the manufacturing of quantum chips/QPUs**
- **Interfaces to at least one EU foundry/pilot line**, and a validation plan
- **Quantitative metrics/targets** demonstrating miniaturisation, integration and manufacturability progress
- Deliver reference designs, design kits or integration notes **enabling reuse across platforms** and uptake by SMEs and pilot lines, with IPR and supply-chain plans ensuring EU access
- Coordinate to onboard relevant digital assets to the **European Design Platform**

# Scope

- Focus on **enabling technologies that support, control, and read out quantum systems** without funding the core quantum chips
- **Target system-level integration and interfaces** and validate solutions in relevant environments, preferably via EU pilot lines/MPWs
- Solutions may include for example:
  - Control and readout electronics across temperature stages including cryogenic
  - Photonic/optical components for routing, modulation, detection and timing
  - Transduction and networking technologies such as microwave-optical conversion
  - Cryogenics, interconnects, packaging and heterogeneous integration for modular assemblies
- Two complementary categories of enabling technologies covered: **Process Enabling Technologies**, and **Operations Enabling Technologies**.
- **Supports enabling subsystems up to pilot-line validation** / MPW tape-out where relevant, in alignment with Chips JU pilot-line access



# Call conditions

- 1 stage RIA topic, co-funded (HORIZON-JU-CHIPS-2026-QUANTUM-2-RIA)
- 7 July 2026 → 17 September 2026
- 20M€ EU budget (expected 5M – 7M per project)
- Participation is limited to legal entities established in EU Member States, EEA countries, Canada, Israel, the Republic of Korea, New Zealand, Switzerland and the United Kingdom

Type of beneficiary	Maximum EU Contribution as % of the Eligible Cost according to HE
For profit organization but not an SME (LE)	50%
SME (for profit SME)	50%
University/Other (not for profit)	50%

# Quantum Design topic outline

Refer to Appendix 8 of Work Programme p. 38

[https://www.chips-ju.europa.eu/GB\\_2025.125\\_Appendix8\\_2026\\_CElv1.pdf](https://www.chips-ju.europa.eu/GB_2025.125_Appendix8_2026_CElv1.pdf)

# Expected outcomes

- A new quantum design facility fully integrated with the European cloud-based semiconductor **Design Platform**, and connected with the **Quantum Pilots**
  - enabling routine MPW/pilot-line submissions by academia, SMEs and Pilot partners
- A validated, interoperable suite of European quantum design tools (including open source) for multiple quantum platforms
- Operational **quantum design flows** and **Quantum Design Enablement Team (QDET)** support, lowering onboarding barriers for pilots and SMEs
- **Common quantum design framework** with harmonized PDK references, shared data/format specifications, and reference libraries
- Standardized workflows, efficient design practices, and **seamless integration with existing semiconductor infrastructure**
- **Consortia to be coordinated by a Research and Technology Organisation (RTO)** with strong experience in quantum hardware-software co-design

# Scope

- Foster a pan-European community around **quantum chip design, building on and closely integrating with the European Design Platform**, in coordination with the Quantum Pilots, European foundries and relevant Design Enablement Teams of the microelectronics sector
- Include research, development, and validation of European quantum design tools
- Progression from community alignment to operational deployment:
  - i. surveying existing quantum design tools and flows, defining common data/models and PDK requirements, identifying components for integration, and preparing reusable libraries and training materials
  - ii. integrating quantum-specific Electronic Design Automation (EDA) capabilities and PDKs into the Design Platform
- **QDET = single-entry point in the Design Platform** for brokerage of MPW shuttles and pilot-line access
- Ensure **interoperability across platforms**, reduce duplication of effort, and **establish a sustainable repository of fully verified and validated** design libraries, models, and toolchain components
- **Establish collaboration channels with foundries and** semiconductor or photonic **pilot lines** to support quantum-compatible fabrication access including training and guidance to designers
- Demonstrate collaboration with other regional, national, or European initiatives
- Expected project duration: **36-48 months**

# Call conditions

- 1 stage RIA topic, co-funded (HORIZON-JU-CHIPS-2026-QUANTUM-1-RIA)
- 7 July 2026 → 17 September 2026
- 30M€ EU budget
- Participation is limited to legal entities established in EU Member States, EEA countries, Canada, Israel, the Republic of Korea, New Zealand, Switzerland and the United Kingdom

Type of beneficiary	Maximum EU Contribution as % of the Eligible Cost according to HE
For profit organization but not an SME (LE)	50%
SME (for profit SME)	50%
University/Other (not for profit)	50%



Please join us this afternoon (13:30 – 16:00) in the Aquarium room for the dedicated Workshop discussing these calls

**Thank you for your attention**