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EVENT**

# YONGATEK Microelectronics

ASIC/FPGA Design and Verification Company

Basri Serdaş

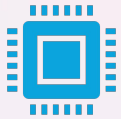
Software Development Director

[basri.serdas@yongatek.com](mailto:basri.serdas@yongatek.com)

# Company at a glance



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Turkiye's  
Chip Design Center



Founded in 2014



70+ People



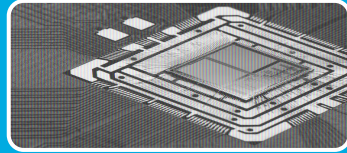
Headquarter : Istanbul  
Office : Ankara



Global Service &  
Delivery 10+ Country

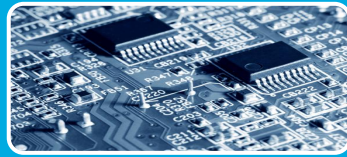


2 patented products



## Digital Design and Advanced Verification

- ASIC & FPGA Design and Verification, RISC-V
- DO-254 Avionics Compliance, Advanced UVM Verification



## Electronic System Design and Verification

- System Architecture and PCB Design, Firmware/Software Design
- System Integration, Test and Verification



## Computer Vision and Real Time Image Processing

- C++ / OpenCV / Cuda / OpenCL Algorithm Development and Optimization
- Hardware implementation on CPUs / GPUs / FPGAs



## Communication

- WLAN, Bluetooth
- SATCOM, 5G, LDPC, MIMO



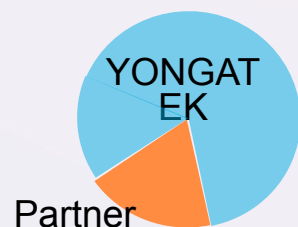
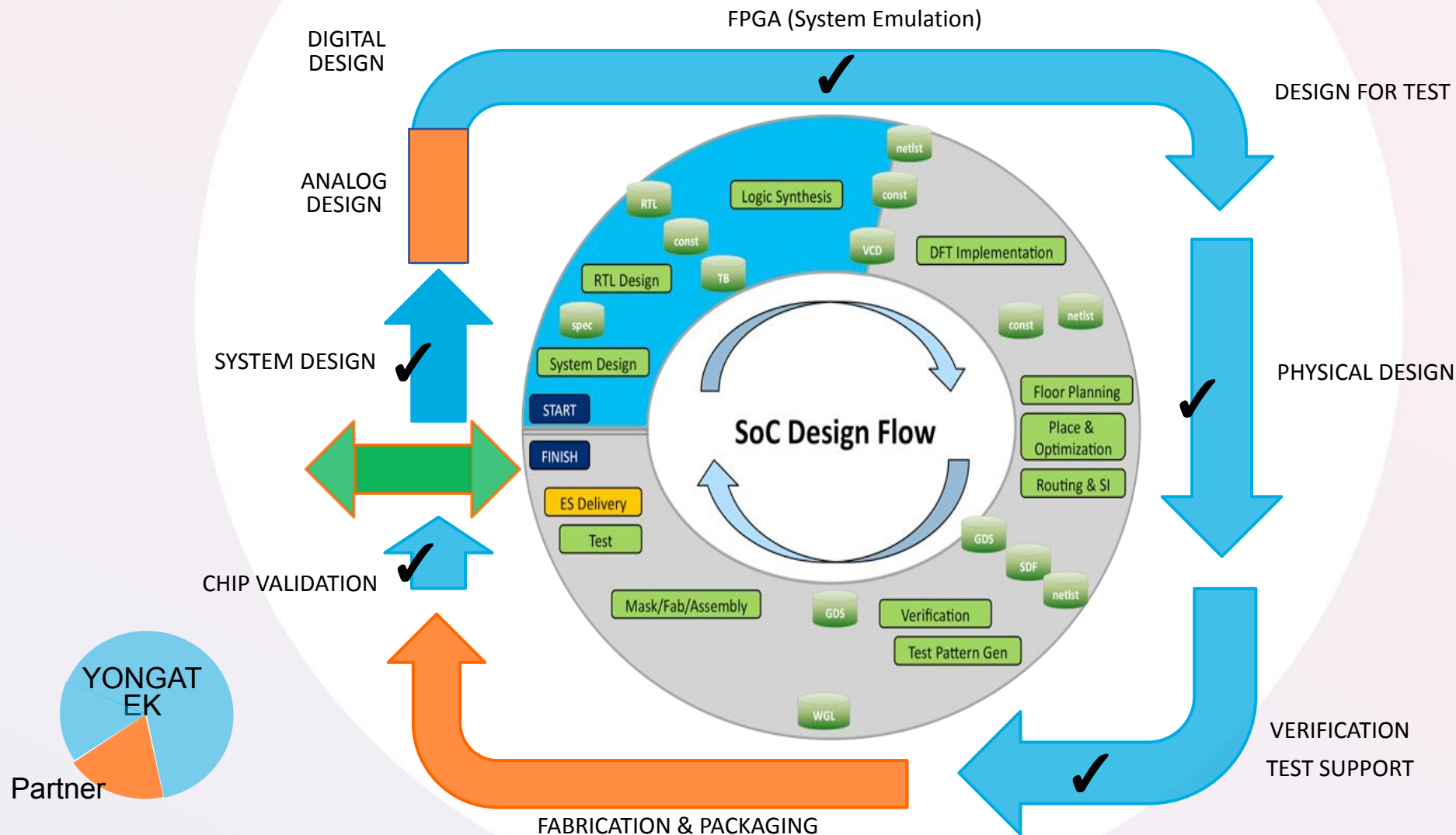
## IoT & Automation

- Preventing Maintenance, Industrial Automation, Quality Control
- Bluetooth, NFC, Lora, RFID, sensor networks

# ASIC Design Competence



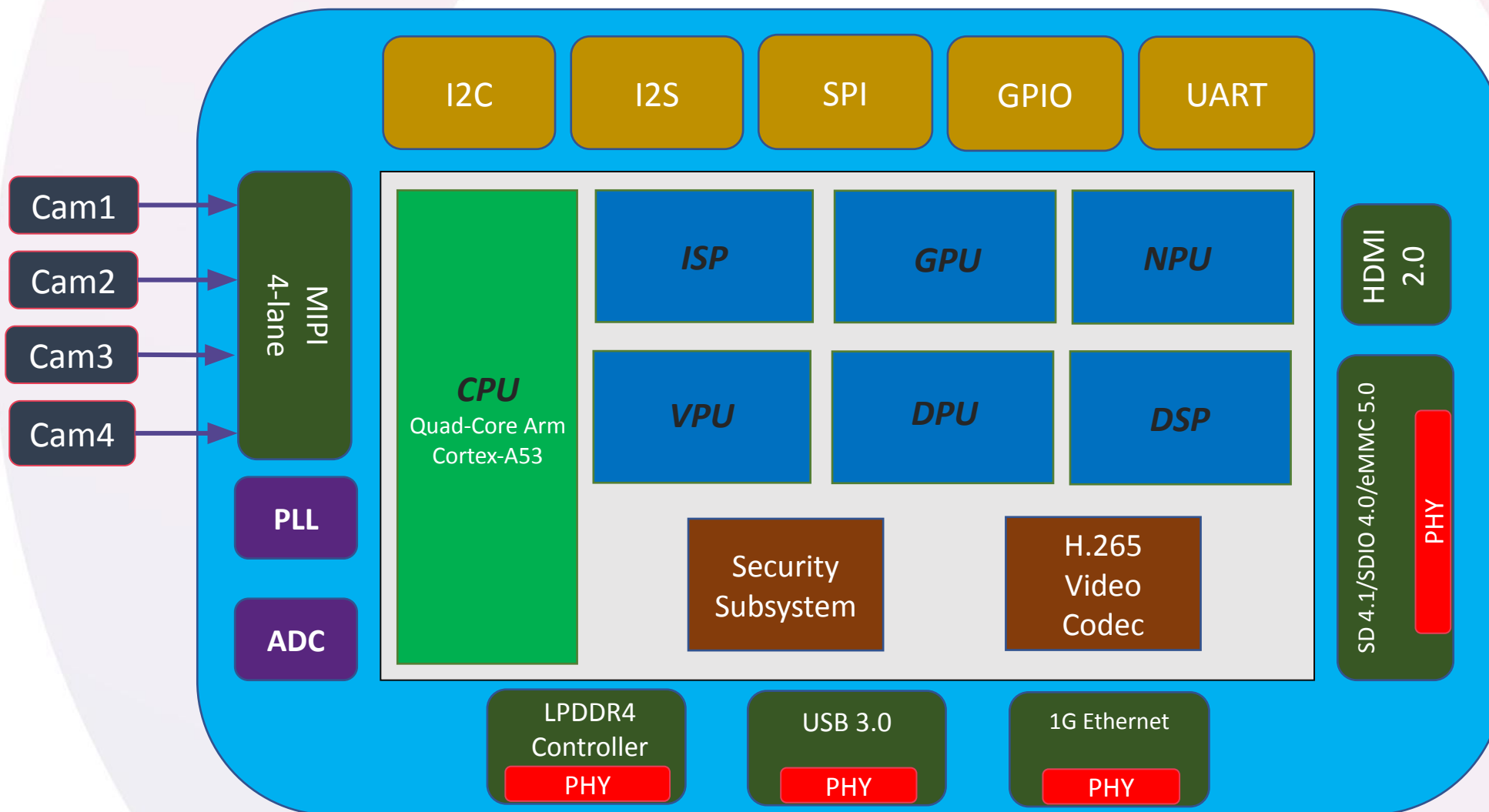
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## Products – KIVA: KIRMIK 2.0 Intelligent Video Analysis SoC



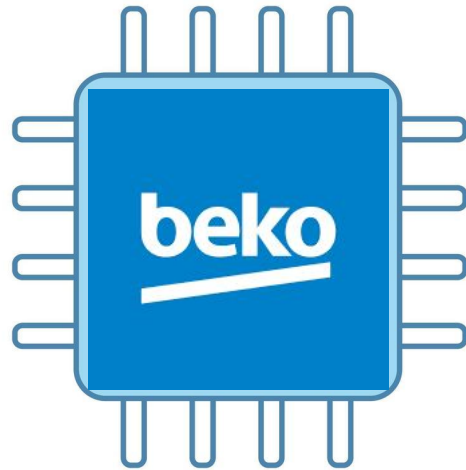
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- AI Based Smart Camera SoC
- TSMC 12 nm
- 4x 4K @30 fps video
- H.265 Video Codec
- 4 core CPU
- ISP, DSP
- NPU, GPU, VPU, DPU
- 4x MIPI interface

Target Tape-out  
@ 2026.Q3

## Products – ÇENTİK RISC-V MCU



- Under design for **BEKO** which is the **largest** home appliances manufacturer company in **Europe**
- TSMC 40 nm
- 30 million chips per year



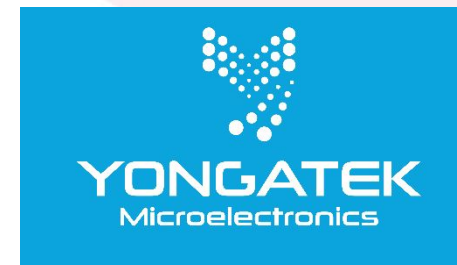
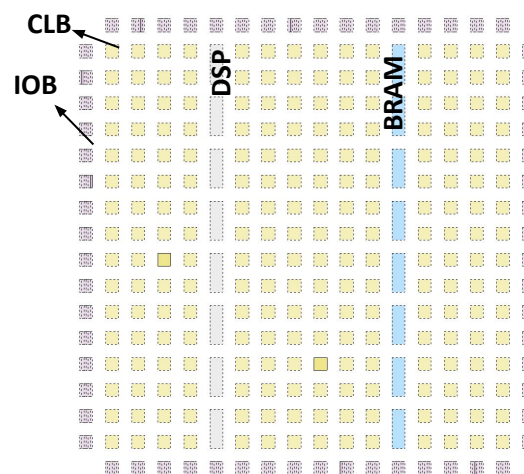
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Target Tape-out  
@ 2026.Q2



## Products – SAKA v1.0: Inhouse Developed FPGA

- RISC-V CPU core
- Heterogeneous architecture with Block RAMs and DSP units
- Block RAM with 1 kB memory units (BRAM)
- 18x18 hard multiplier units (DSP)
- TSMC 40 nm technology production
- 16x16 Tile-Based Complex Logic Block (CLBs)
- 8 Logic Elements (LE) inside each CLB
- 4-input Look-up Table (LUT4) and FF inside each LE
- Fracturable LUTs to allow multi-output in LUT
- ~400 General-Purpose I/Os
- OpenFPGA EDA framework for Synthesis, STA, P&R and bitstream generation
- Benchmarking through numerous RTL designs



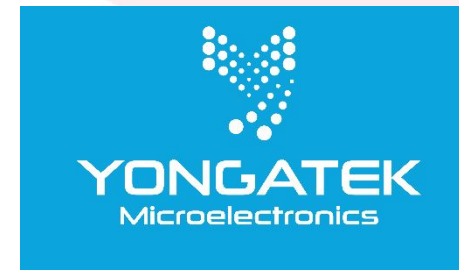
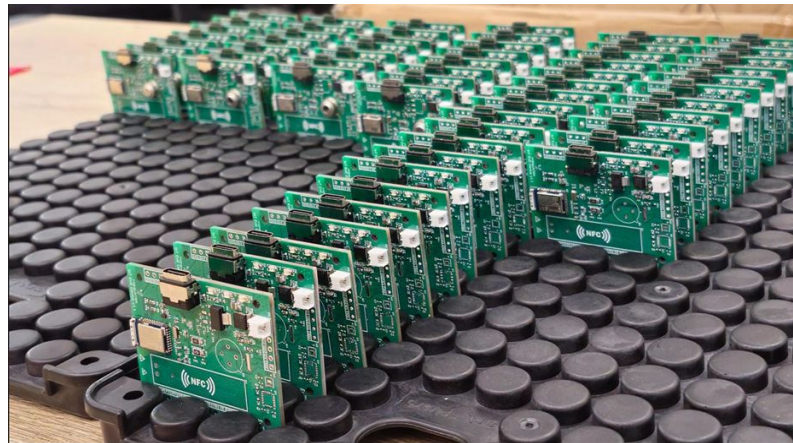
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Target Tape-out  
@ 2026.Q2

## Products – FABIoT: AI-Driven Predictive Maintenance System

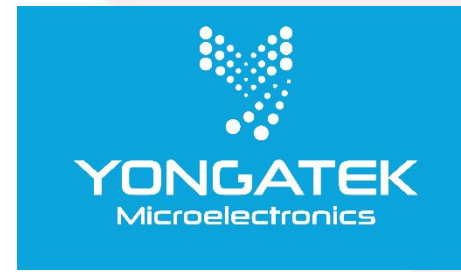
- Integrated multi-sensor data (temperature, humidity, vibration, magnetic, RFID, ultrasound, camera etc.) with
- Bluetooth and NFC connectivity
- Wi-Fi/4G/5G gateway access,
- AI-driven cloud-based predictive intelligence for automatic decision-making and real-time performance optimization.
- Use Cases;
  - Conveyor Belt Health Monitoring
  - Industrial Automation for manufacturing



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# Company's Activities



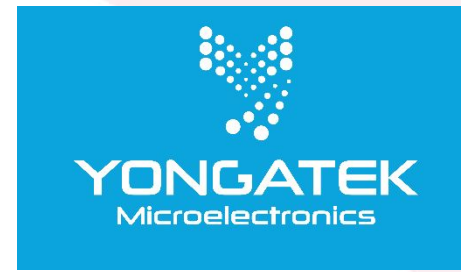
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- Is there any previous experience with collaborative projects?
  - **TRISTAN** (2022-2026) – WP Leader
  - **LoLiPoP IoT** (2023-2026)
  - **RIGOLETTO** (2025-2028) – WP Leader
- What sort of interaction exists with one of the 3IAs or other ETPs?
  - Member of EPoSS
  - Member of EPoSS/INSIDE Edge AI Working Group





# Collaboration Expectations



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Collaborative project of interest to you

*Chips JU, Horizon Europe, Eureka Clusters and Eurostars*

Scope

*ASIC/FGPA Design/Verification and Embedded Software Development for many domains like AI, Communication, Computer Vision, Cyber Security, IoT.*

Project idea

Project impact

Project consortium

*We are eager to be part of project(s) where we can create value with our expertise*



Contact:

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**THANK YOU**