Status of the Chips for EU Initiative

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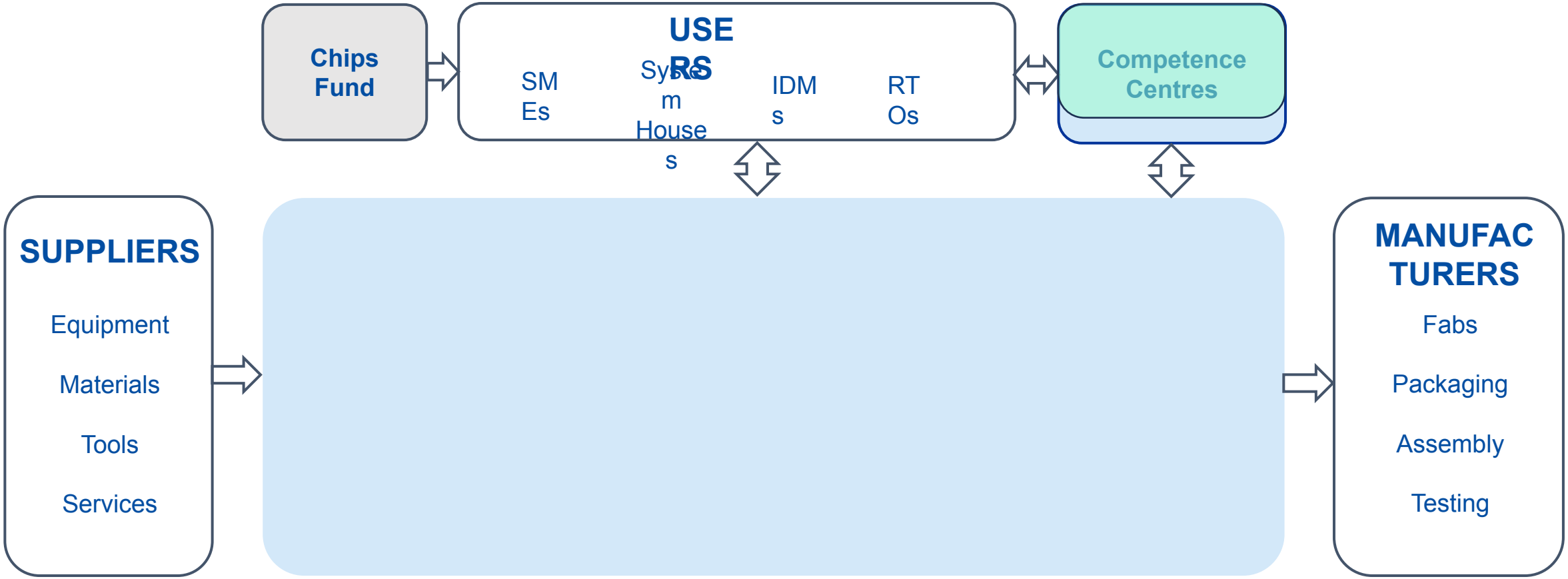
EUROPEAN PARTNERSHIP

Ongoing Activities Chips for Europe Initiative Part

Chips for Europe Initiative	HE Budget	DEP Budget
Operational budget	**1,417 M€**	**1,373 M€**
Signed contracts	761 M€	720 M€
In preparation	133 M€	331 M€
Total	**894 M€**	**1,051 M€**

Chips for Europe Initiative



Pilot Lines

- NanoIC

  The overall objective of the NanoIC project is to set up and give access to a 300mm pilot line to the entire semiconductor ecosystem to advanced, beyond 2nm system-on-chip technologies.

- FAMES

  With the goal of transferring results to the EU semiconductor industry, the FAMES Pilot Line will develop advanced technologies offering 2 generations of FD-SOI at 10nm and 7nm nodes.

- APECS

  Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems Pilot Line (APECS-PL).

- WBGPL

  WBGPL aims to realise an integrated pilot line focused on the developments of the wide-bandgap (WBG) semiconductors technologies for power and radio frequency (RF) electronics. PIXEurope

- PIXEurope

  PIXEurope will establish a globally unique Open Access Pilot Line, addressing key technological and production challenges associated with Photonic Integrated Circuits (PICs)

Competence Centres & Design Platform

- CCC1

  Have specialised areas of expertise in certain technology, domain, or activities (specialisation). Facilitate effective use of capacities and facilities, including access to design platform and pilot lines. Support interested stakeholders in developing semiconductor solutions (technology transfer). Address skills shortage by offering (access to) training on semiconductors, including workforce upskilling and reskilling. Match user needs with available expertise in network of competence centres and act as access point to the network, Awareness raising, promoting services, promoting success stories

- CCC2

  Targeting the establishment of European Network of Chips Competence Centres (ENCCC)

- CCC3

  Additional call for competence centers for countries that did not submit in the first call

- PCT

  The DECIDE project aims to create a virtual design platform to democratize access to advanced semiconductor technologies across Europe. This platform will support the innovation and competitiveness of European startups, SMEs, and research institutions. By integrating Design Enablement Teams (DETs), the platform will offer customized support, access to Electronic Design Automation (EDA) tools, intellectual property (IP), and pilot line technologies, helping Europe to deploy next-generation semiconductor technologies rapidly

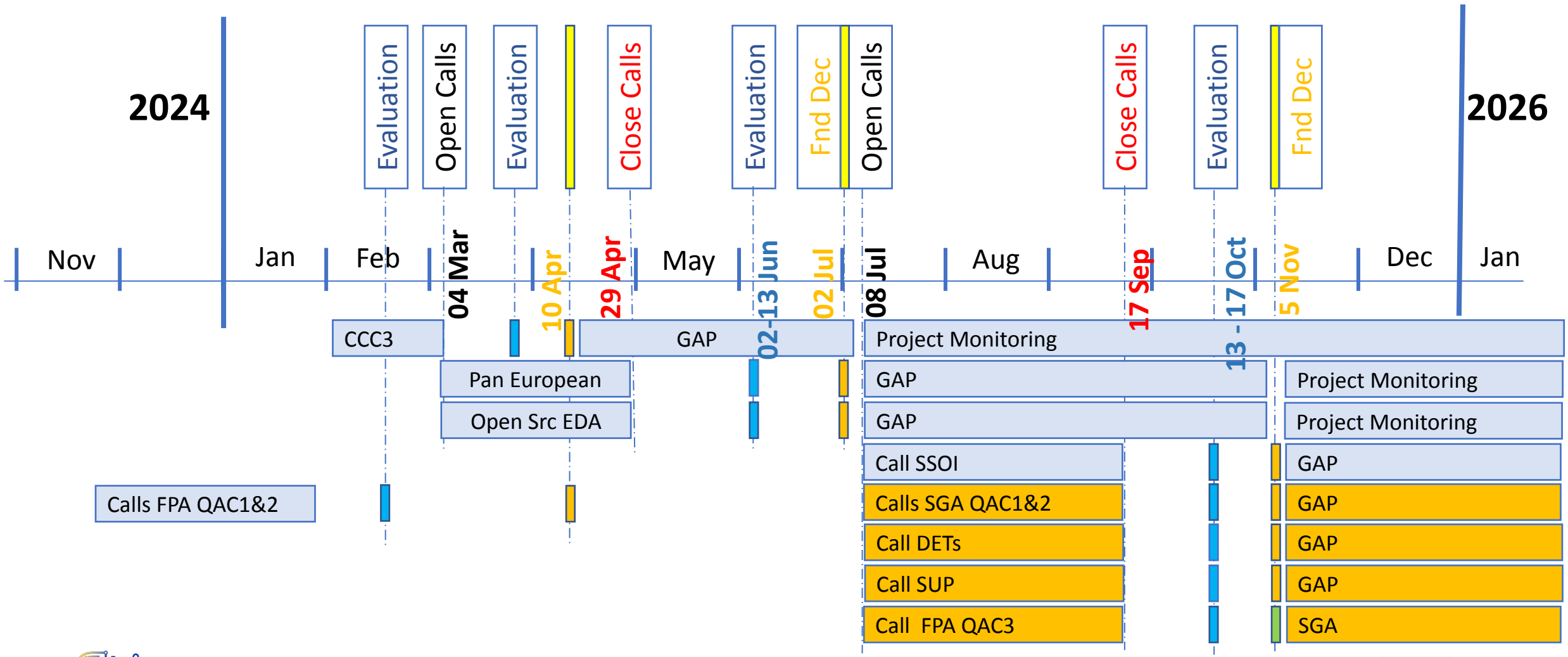
HE Actions 2025

Topic	Description	Indicative JU Budget M€
HORIZON-JU-Chips-2025-RIA-SUP	Support for start-ups and SMEs	**220**
HORIZON-JU-Chips-2025-CSA	Pan-European infrastructure for Chips Design Innovation	**12**
HORIZON-JU-Chips-2025-IA-EDA	Open-source EDA tools development	**20**
HORIZON-JU-Chips-2025-FPA-QAC3	Establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots	**0**
Lab to Fab	Lab to Fab accelerator European ecosystem for chiplet integration	**50**
Other Activities		
HORIZON-JU-Chips-2025-SGA-QAC1	Supporting developing Quantum Chip Technology for stability Pilots	**50**
HORIZON-JU-Chips-2025-SGA-QAC2	Supporting developing Quantum Chip Technology for high-quality Trapped Ions Pilot	**20**
TOTAL		**372**

DEP Actions 2025

Topic	Description	Indicative JU Budget M€
Call for tenders	Cloud platform for the European Design Platform	**15**
DIGITAL-JU-Chips-2025-CSA-DET	Set-up and integration of Design Enablement Teams	**5**
DIGITAL-JU-Chips-2025-SG-SSOI	Accelerator for Advanced Strained Silicon on Insulator Substrates	**30**
DIGITAL-Chips-2025-1-IA-LEAI	Low-power Edge AI Chips	**20**
TOTAL DEP		**70**
TOTAL Chips for EU Initiative 2025		**442**

Planning Calls 2025



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