The APECS pilot line – European chiplet innovation

How APECS leads the way in heterogeneous integration by providing diverse design capabilities, technologies and testing strategies for electronic components and systems on a single platform

What are the challenges in heterogeneous integration?

Design complexity

- Integrating different materials (CMOS, InP, GaAs, SiPh)
- Managing electrical and optical coupling
- Ensuring co-design efficiency and thermal stability

Standardization

- Defining universal design rules
- Standardizing interfaces
- Ensuring process compatibility
- Establishing reliability benchmarks

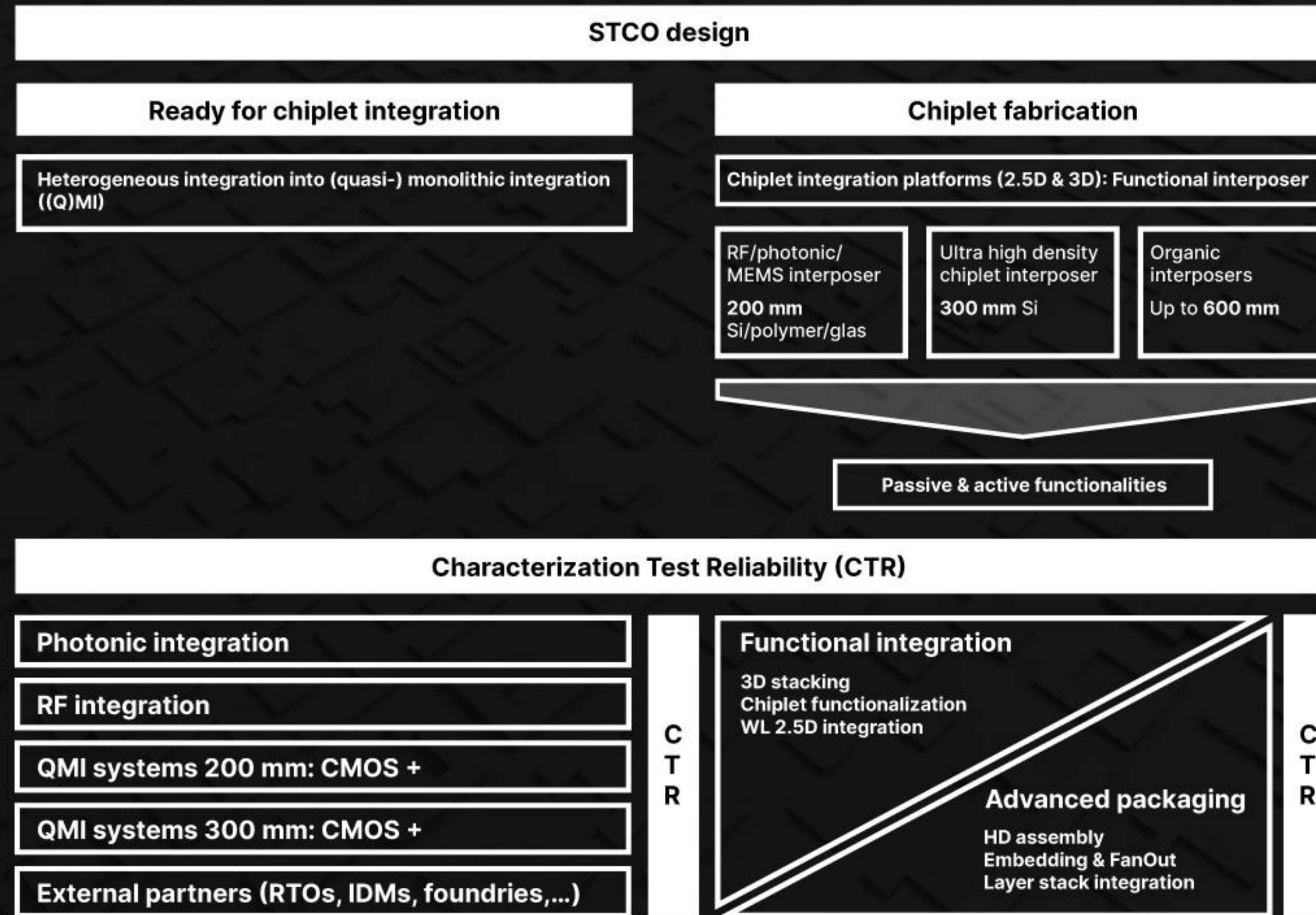
Manufacturing precision

- High density interposers (organic/inorganic)
- Sub-micron alignment
- Controlling process variations
- Enabling stress-free bonding
- New testing concepts

Cost management

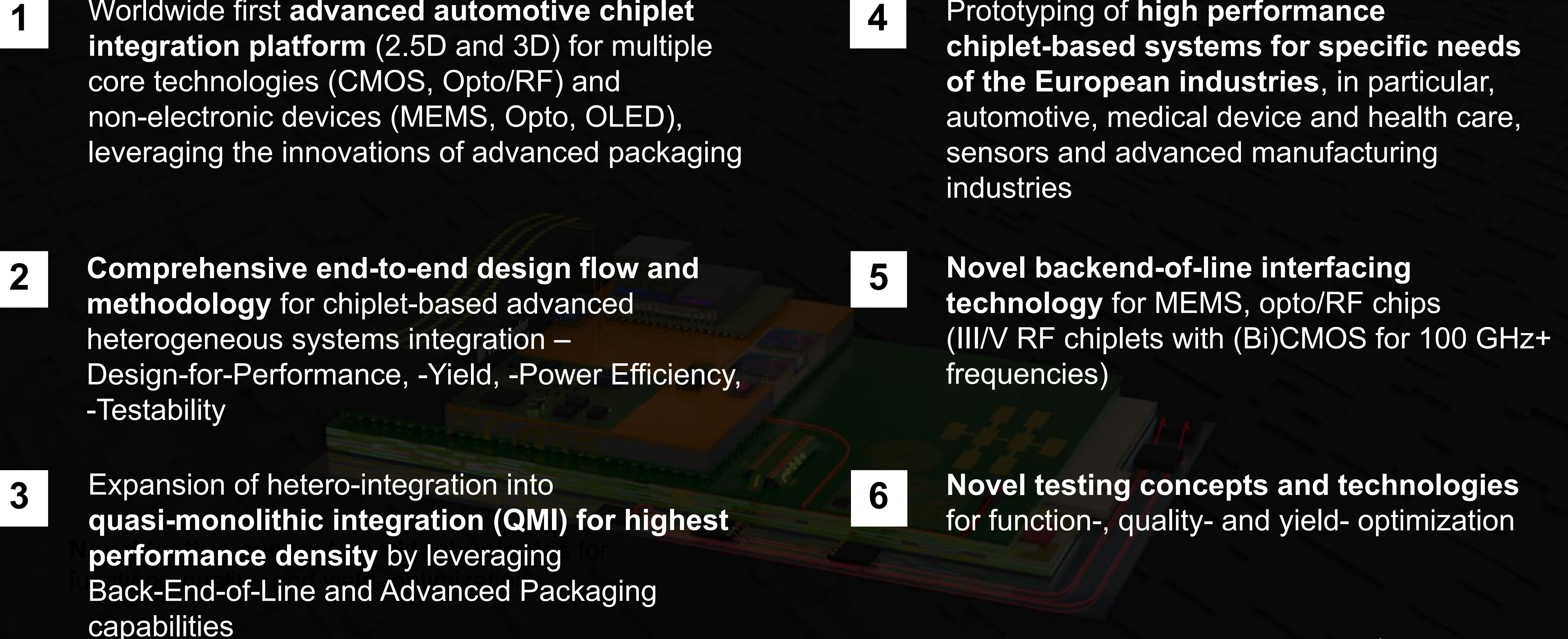
- Reducing fabrication costs
- Improving yield
- Scaling automated assembly
- Minimizing supplier dependency

APECS brings the connection between design, technology and testing for wide range of applications



APECS

Key innovations of the APECS pilot line



1 Worldwide first **advanced automotive chiplet integration platform** (2.5D and 3D) for multiple core technologies (CMOS, Opto/RF) and non-electronic devices (MEMS, Opto, OLED), leveraging the innovations of advanced packaging

2 **Comprehensive end-to-end design flow and methodology** for chiplet-based advanced heterogeneous systems integration – Design-for-Performance, -Yield, -Power Efficiency, -Testability

3 Expansion of hetero-integration into **quasi-monolithic integration (QMI) for highest performance density** by leveraging Back-End-of-Line and Advanced Packaging capabilities

4 Prototyping of **high performance chiplet-based systems for specific needs of the European industries**, in particular, automotive, medical device and health care, sensors and advanced manufacturing industries

5 **Novel backend-of-line interfacing technology** for MEMS, opto/RF chips (III/V RF chiplets with (Bi)CMOS for 100 GHz+ frequencies)

6 **Novel testing concepts and technologies** for function-, quality- and yield- optimization

APECS

Application areas of the APECS pilot line

High performance computing

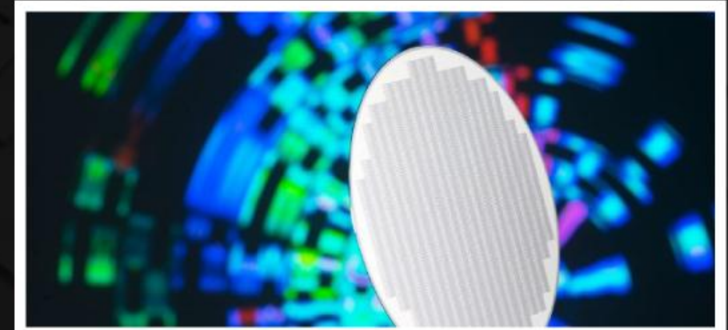
Medical & scientific instrumentation

Sensor systems

Telecommunications

Industrial manufacturing

Artificial intelligence (AI / ML)



Purpose of the APECS pilot line

- Position **Europe´s R&D and industry at the forefront of semiconductor innovation**
- Establish a **cutting-edge infrastructure** for heterogeneous integration and chiplet technology
- Advance **technological capabilities for cutting-edge semiconductor devices**
- **Support European industries** (e.g., automotive, telecom, healthcare, IoT)
- **Join forces with Europe's RTOs** to accelerate technology transfer and enhance collaboration among

Join forces with Europes´ leading RTOs

VTT: IPD and RF on silicon and glass substrates; Heterogenous 3D integration: ALD for TSV and Wafer Level and LTCC Packaging of RF and optical MEMS

imec: RDL 1st Chiplet Packaging Demonstrator and Chiplet Integration Package

CEA-Leti: FOWLP technology for RF (>150GHz) System-in-Packages (SiP) and Glass substrates for > 100GHz RF passive component

TU Graz: ESD for heterogeneous integration

INL: 3D heterogenous integration of graphene FET biosensors

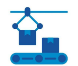
CNM/CSIC: Microchannel cooling, Printed antennas

FORTH: 3D Sequential Integration (3D SI) of GaN based RF front end (RFFE) chips

Potential for industrial uptake

Users

Chip Foundries


Integrated Device Manufacturer (IDMs)

Materials & Tools Supplier

Semiconductor Customer

Research Community

Start-ups

Value Proposition

Design Services: enable chip, chiplet IP, and system design for APECS Pilot Line; provide and operate design platforms with support

Process development, materials and tool validation: accelerate technology development and validate processes for commercial transfer

System Development: leverage APECS tech for new products and business; enable access to specialized technologies

Manufacturing Outsourcing: offer Proof of Concept, prototype runs, small-volume production, and scalable transfer options

Design Services: enable chip, chiplet IP, and system design for APECS Pilot Line; provide and operate design platforms with support

Research Access: support research-to-application transfer; Provide easy access via local competence centers

Benefits for the European semiconductor ecosystem

Increased competitiveness in the global semiconductor market

The APECS pilot line strengthens Europe's position in the global semiconductor market by enabling cutting-edge design and advanced manufacturing.

Economic growth via job creation and high-tech investment

Facilitating high-tech investments in manufacturing infrastructure and increasing skilled workforce development for sustainable job creation in Europe.

Building supply chain resilience by creating local capabilities

Localizing key semiconductor capabilities mitigates dependency risks and ensures a stable supply chain.

Accelerated innovation through faster development cycles

Faster prototyping and validated process transfers reduce time-to-market for new semiconductor technologies.

Coordinated by

Implemented by

Pilot Line Project Partners

Co-funded by

APECS is co-funded by the European Commission and national ministries of the eight member states within the framework of the EU Chips Act. Overall funding for APECS amounts to € 730 million over 4.5 years.

APECS

APECS