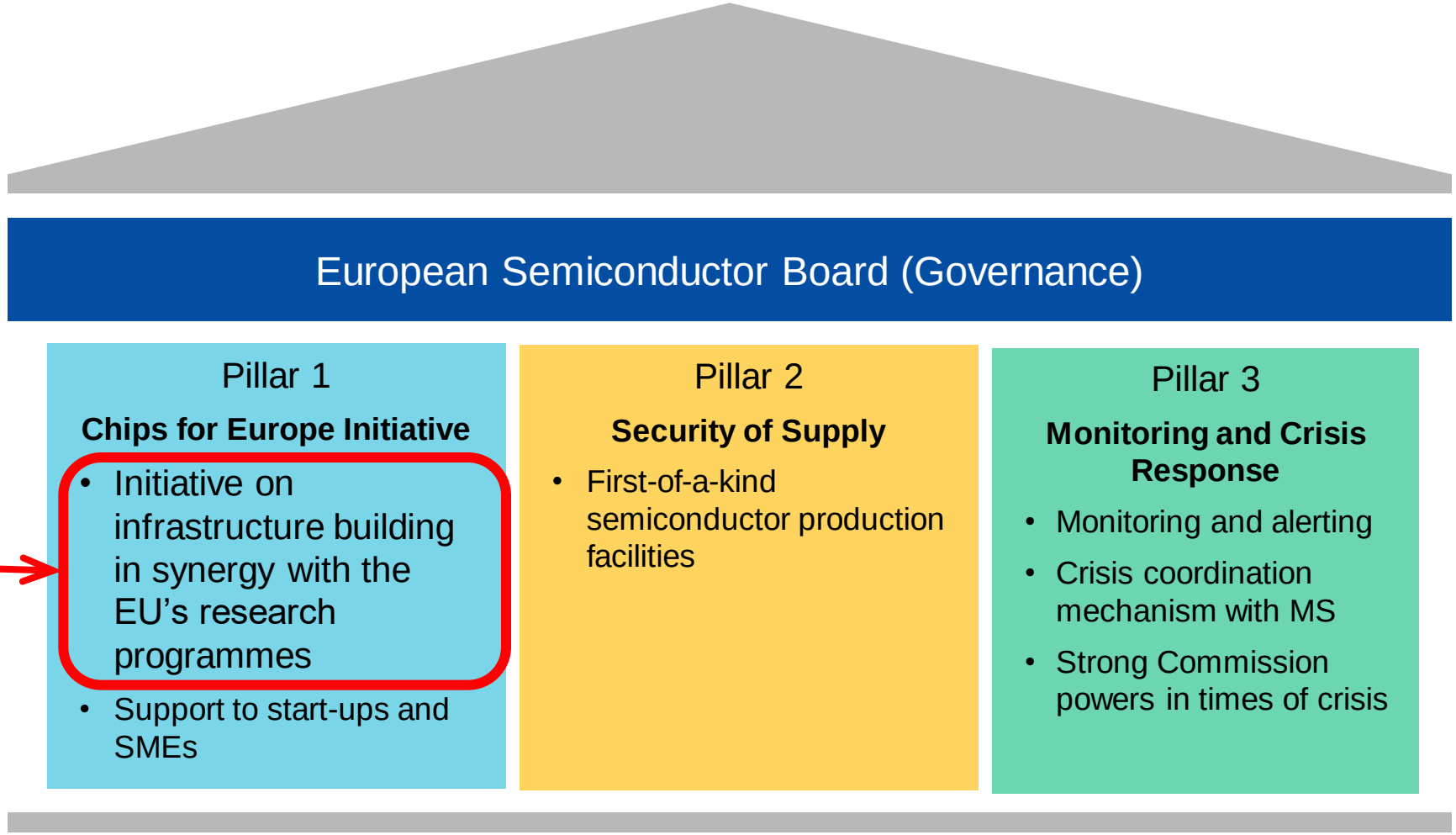
Chips JU Initiative calls 2023 and 2024

Yves Gigase
Head of Programmes
21 February 2024

EUROPEAN PARTNERSHIP

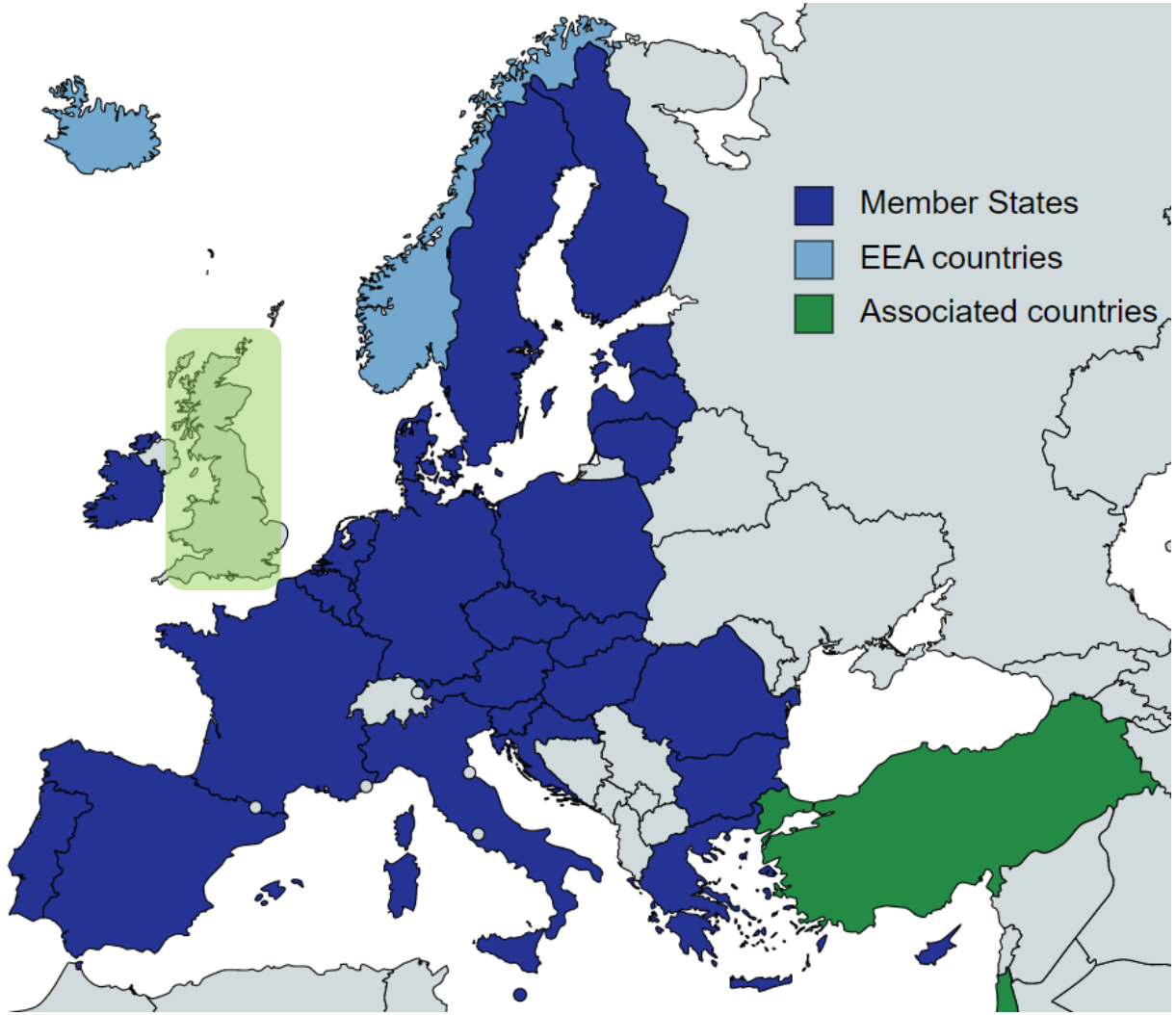
The 3 pillars of the Chips Act



Chips JU objectives

a) Reinforce EU strategic autonomy in electronic components and systems
b) Establish EU scientific excellence and innovation leadership
c) Ensure that components and systems technologies address Europe's societal and environmental challenges
d) Pilot lines
e) Design platform
f) Competence centers
g) Quantum chips technology
h) Skills

→ **INITIATIVE**



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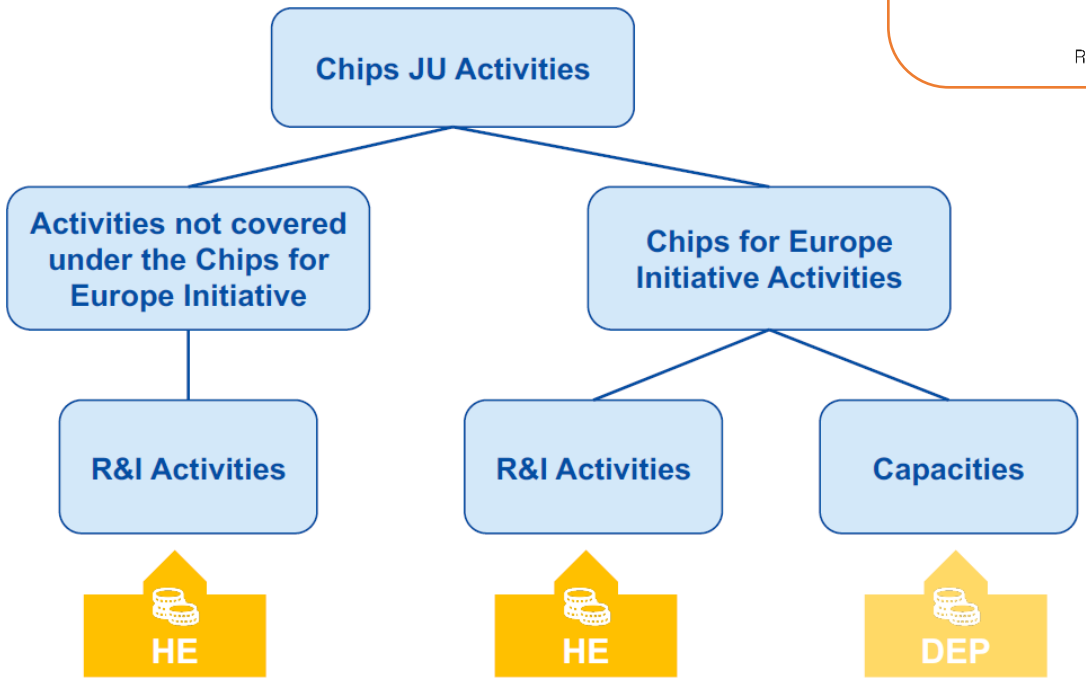
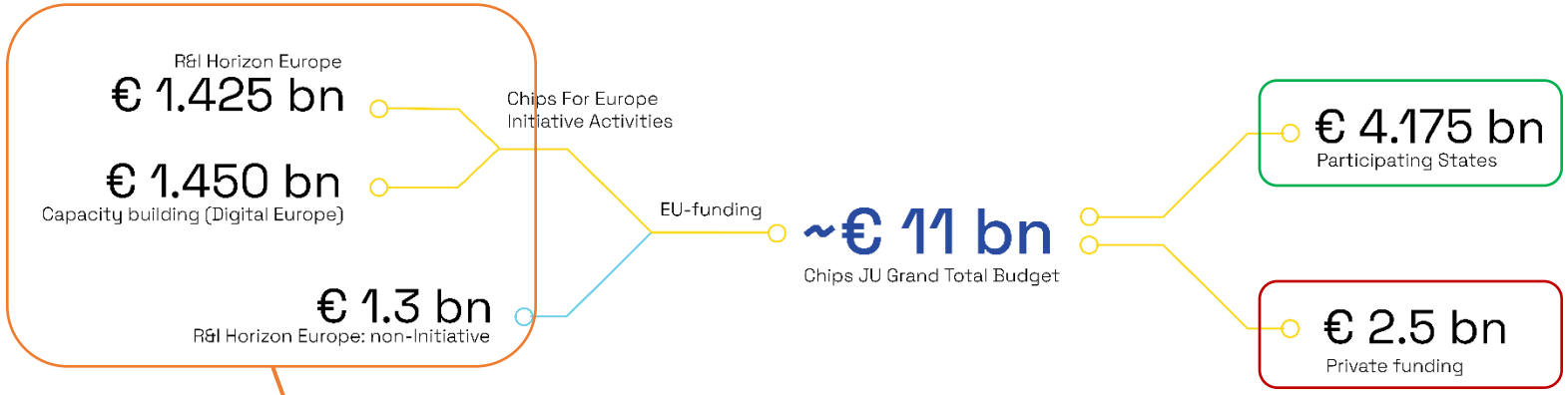
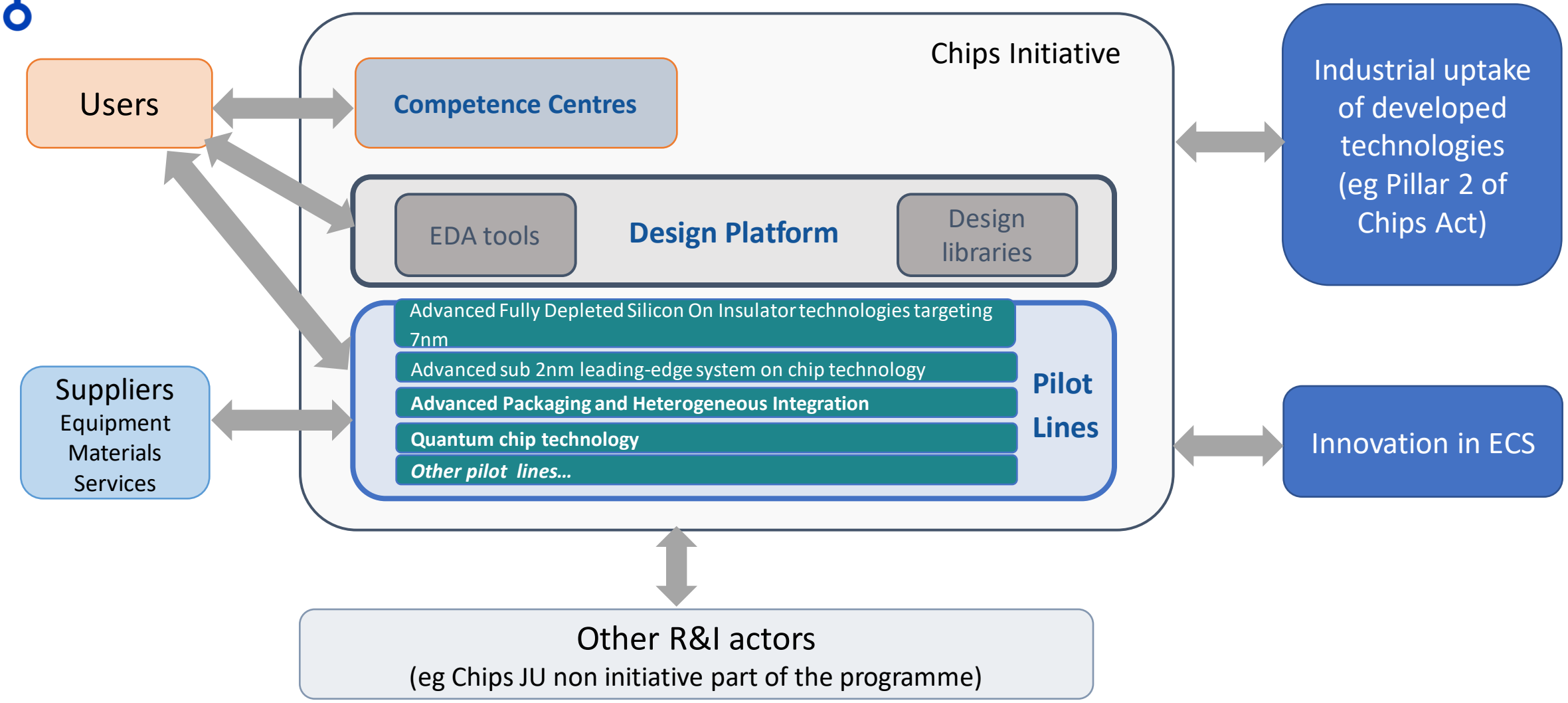
Chips JU Funding





EU Contribution to Chips JU (excl	Chips for Europe Initiative	Non-Initiative	Total
R&I (Horizon Europe)	1.425	1.300	2.725
Cap building (DEP)	1.450	n.a.	1.450
Total	**2.875**	**1.300**	**4.175**

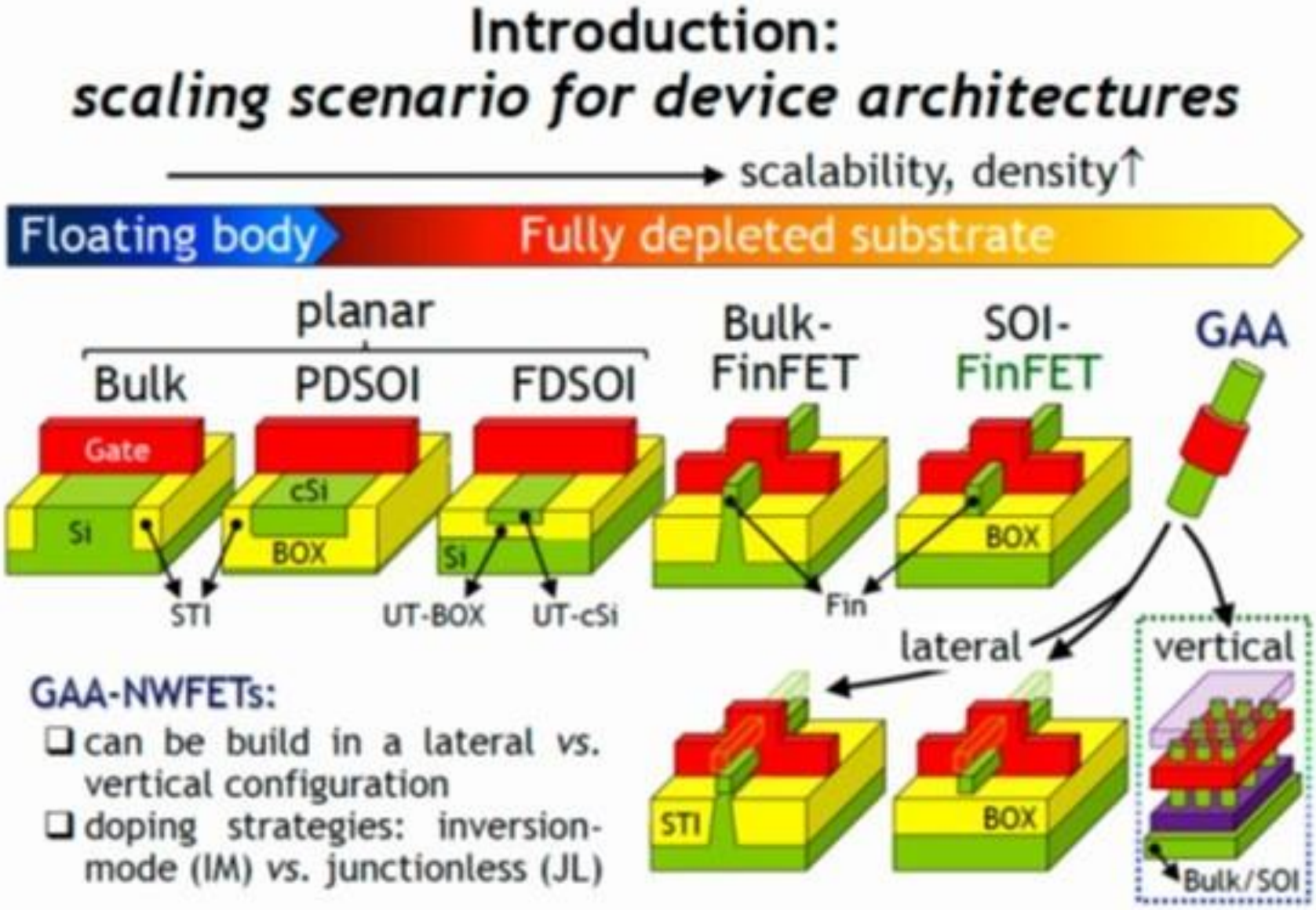
Chips JU: From Lab to Fab



Call Chips 2023: First calls opened in Dec. 2023

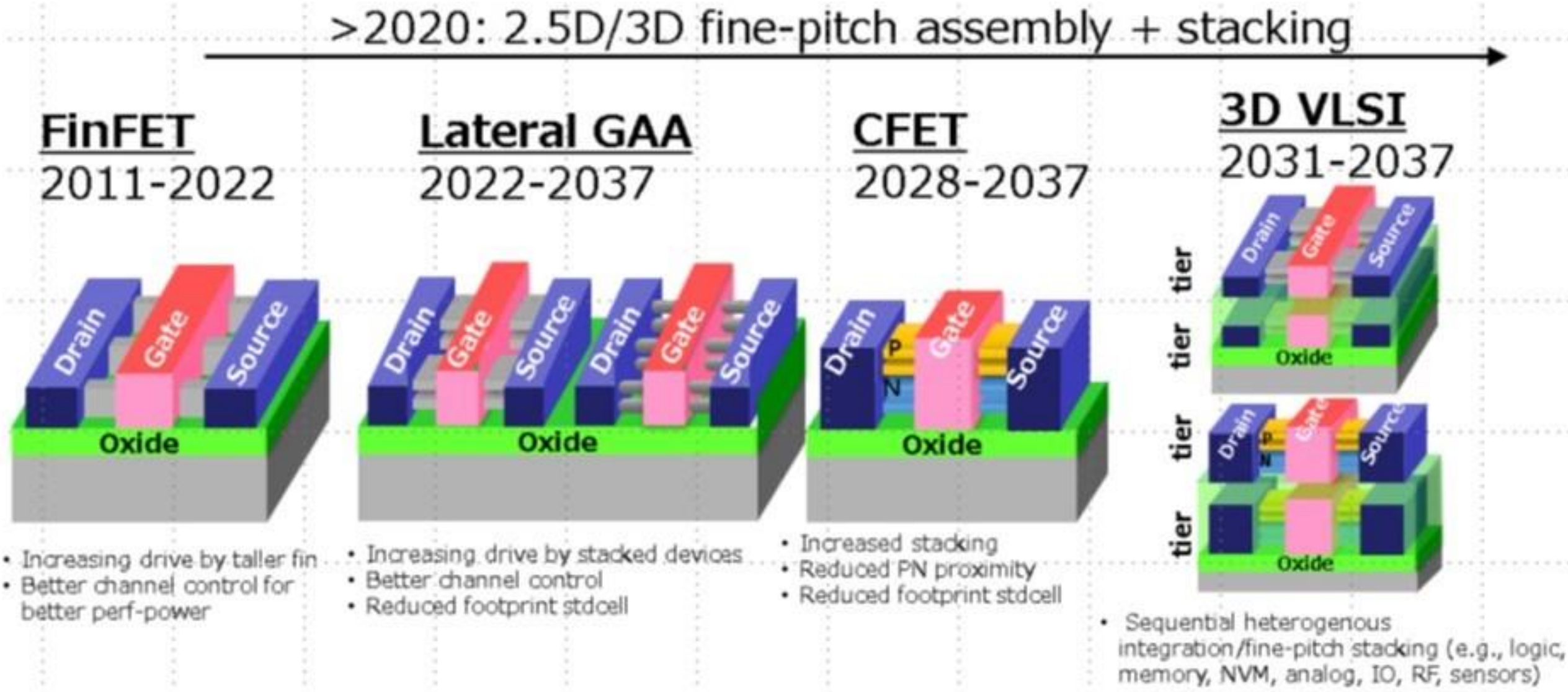
Call	Topic	Max EU Contribution	Participating States' contribution	Total
Chips-CPL-1	Pilot line on advanced sub 2nm leading-edge system on chip technology	700 MEUR	700 MEUR	1,400 MEUR
Chips-CPL-2	Pilot line on advanced Fully Depleted Silicon On Insulator technologies targeting 7nm	420 MEUR	420 MEUR	840 MEUR
Chips-CPL-3	Pilot line on advanced Packaging and Heterogenous Integration	370 MEUR	370 MEUR	740 MEUR
Chips-CPL-4	Pilot line on advanced semiconductor devices based on Wide Bandgap materials	180 MEUR	180 MEUR	360 MEUR

- Closing date February 29, 2024. Complex call starting with a Call for Expression of Interest leading to a Hosting Agreement and a Joint Procurement Agreement, and calls for related HE and DEP grants.
- Expected project start in 2Q 2024.

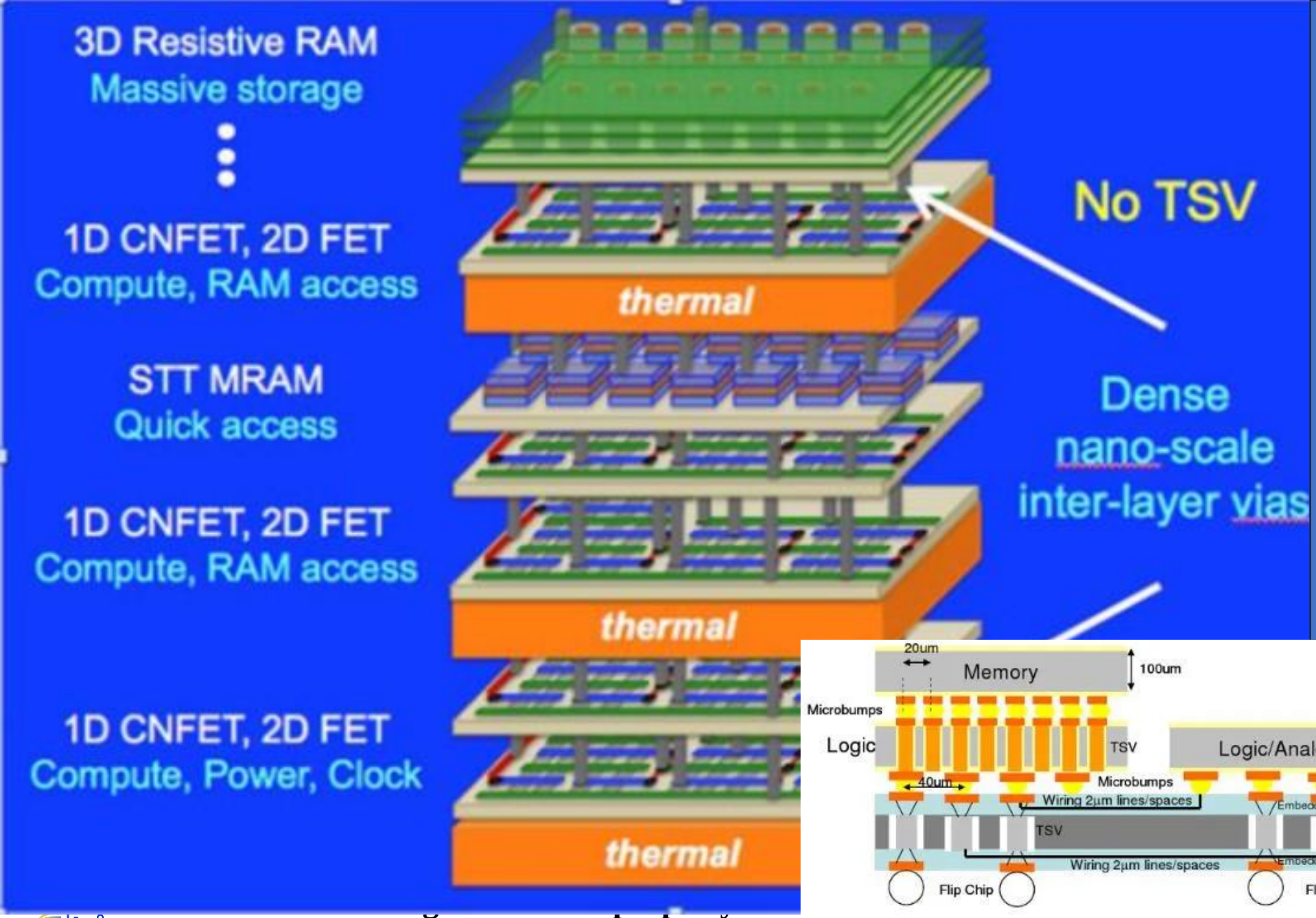


IRDS roadmap 2022 Executive summary

Figure ES56 Practical migration of transistor structure from FinFET to GAA to fully vertical



IRDS roadmap 2022 Executive summary ***Figure ES57 Change in the MOSFET device architecture from the 2D planar through 2.5D FinFET to 3D monolithic VLSI with GAA***



IRDS roadmap 2022
Executive summary
Figure ES58 Planning for the advent of monolithic heterogeneous integration

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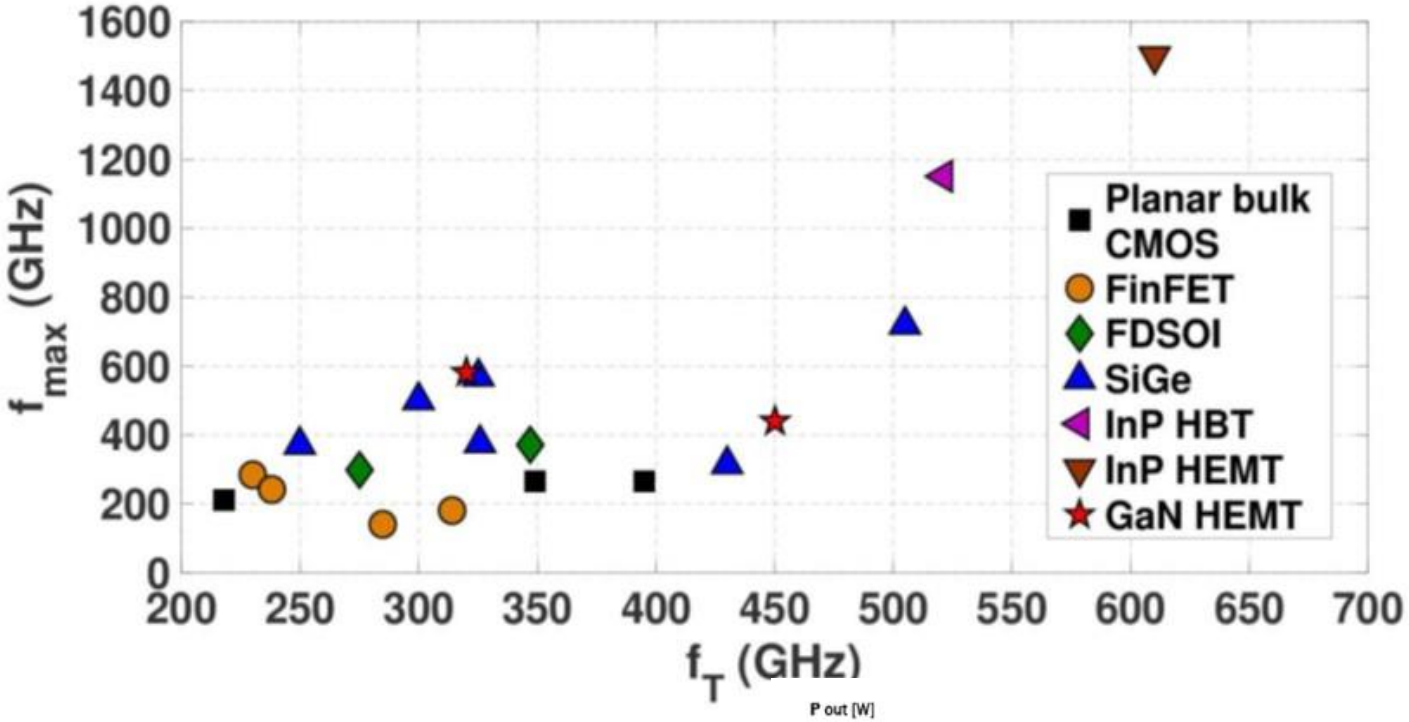
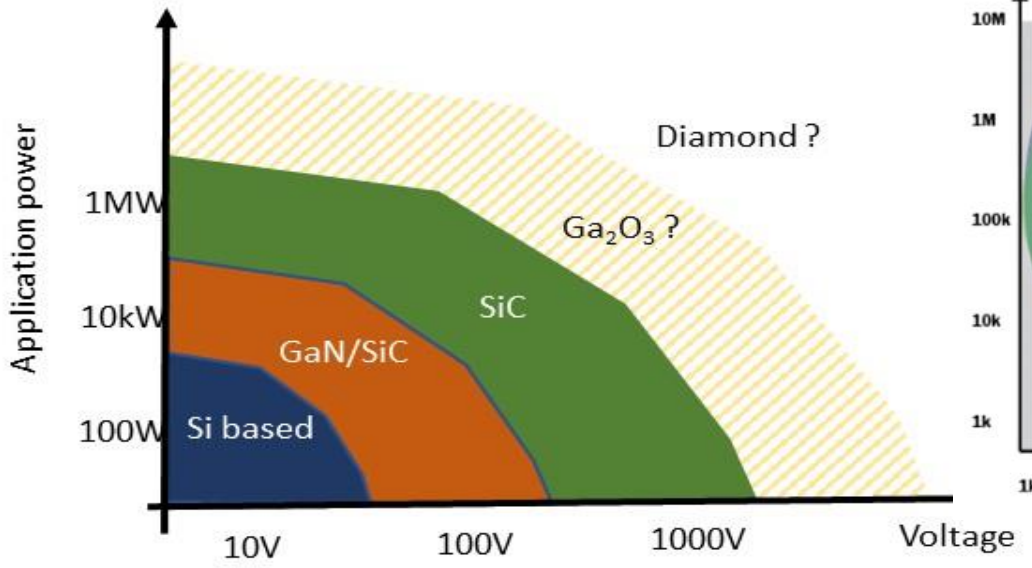
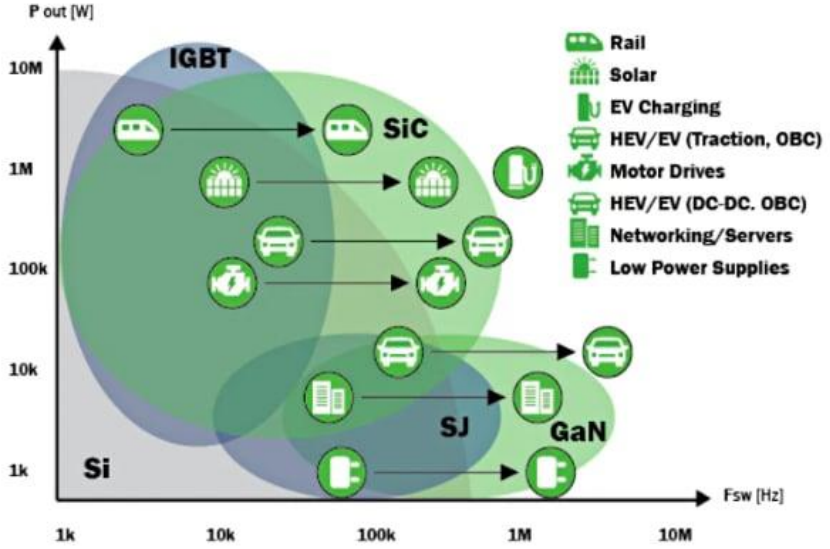






IRDS roadmap 2022
Executive summary

Figure ES46 Silicon device limitations to operate above 400 GHz

Some general outcomes common to all PL

- **Expanding the European user base** of this technology and build a community of interest around this technology.
- **Access** to those advanced technologies, **preferential for SMEs and Start-ups** with the **support of the Competence Centers** to be started by the Chips JU.
- Early research **Process Design Kits for the design platform** and support to the design platform for those kits.
- A **collaboration with the other pilot lines** established under the Chips JU, **creating a strong networked European environment for advanced chip technologies.**
- **Training and skill development**

Call Chips 2024: Initiative part

Call	Topic	Max EU Contribution
Chips-2024-CDP-1	Design platform. A cloud-based virtual platform that will enable users, particularly academia, start-ups and SMEs, to design and develop their chips	330 MEUR
Chips-2024-CPL-5	Additional pilot line(s);	180 MEUR
Chips-2024-CQC-1	Quantum chips technology (preparatory action for a pilot line)	30 MEUR
Chips-2024-CCC-1	Competence centres. The centres are tol provide access to technical expertise and experimentation in the area of semiconductors, helping companies, SMEs in particular, to approach and improve design capabilities and developing skills. Max 1 per Participating State, funding up to 1 MEUR/yr from the EU for 4 years, to be matched nationally. Restricted call after national processes.	116 MEUR
Chips-2024-CCC-2	European Network of Chips Competence Centres (CSA)	4 MEUR

WHAT WOULD HELP ?

Access to a repository of IP (both open source and commercial)

Easy access to design tools with reduced contract negotiation time

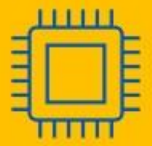
Tool-oriented and practical training

Customised cloud instance with scalable compute + storage resources

Application engineering support (design enablement)

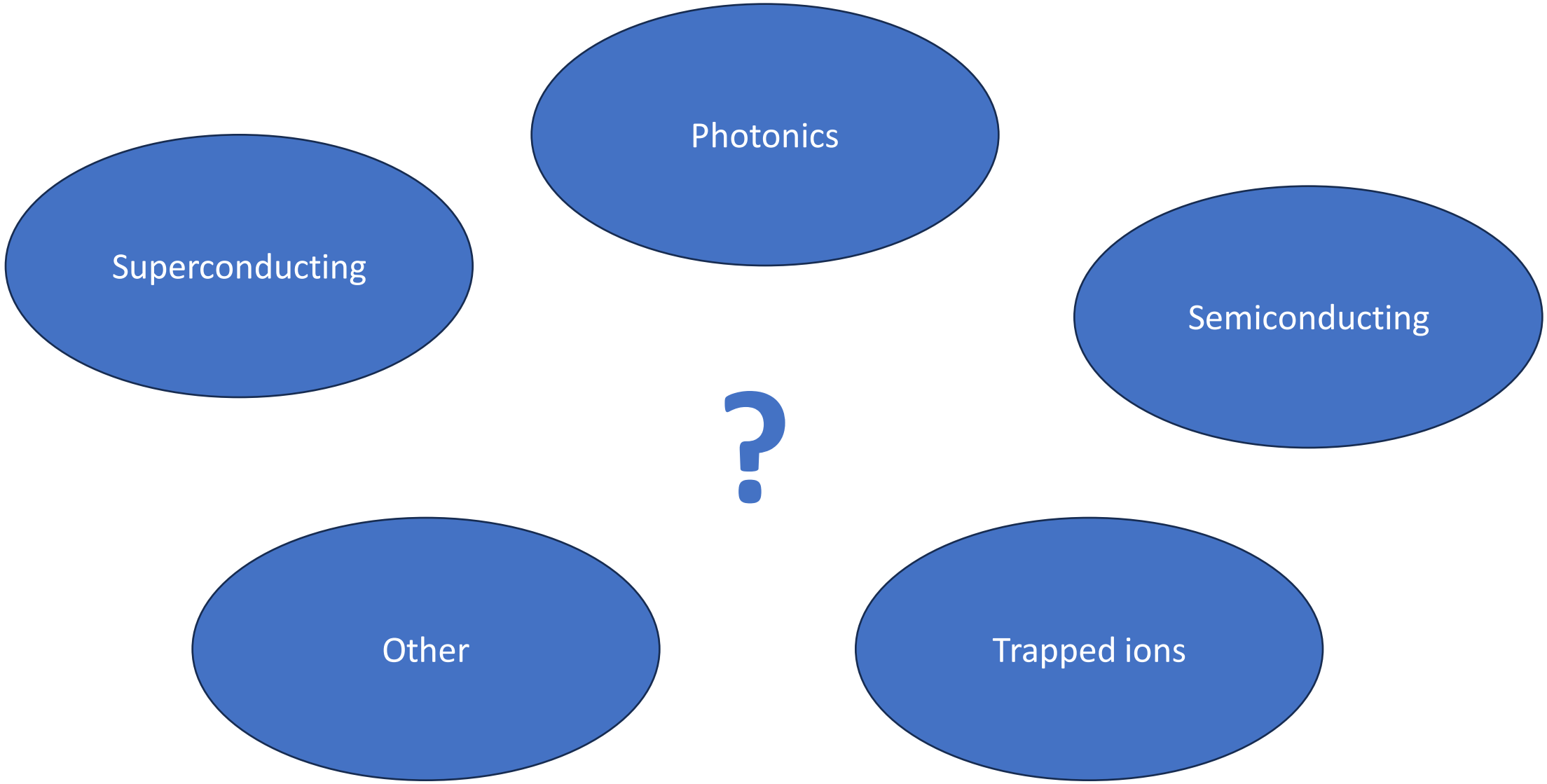
EDA tools and IP sandbox (community-based testing + valid.)

Access to pilot line and foundry PDKs/ADKs



Support until first prototype (MPW)

Ambition: to provide start-ups, SMEs and other users a design environment similar to what is expected at larger companies through the aggregation of demand


Photonics
Superconducting
Semiconducting
?
Other
Trapped ions