CHIPS JOINT UNDERTAKING

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EUROPEAN PARTNERSHIP

WHAT IS CHIPS JOINT UNDERTAKING?

Public-private partnership (PPP)

Partnerships between public authorities and industry intend to bring project results closer to the market and improve the link between research and societal growth. The PPPs are based on long term contracts that can take many different legal forms, from contractual partnerships to specific legal entities.

Joint undertaking (JU)

A Joint Undertaking is an institutionalized PPP with its own legal identity, with its own governance, budget etc.. In most cases, like for the Chips JU, the JUs are established by an EU regulation called the Single Basic Act which defines what the JU has to do and how it must do it. Most of the rules governing the JUs are very similar to those of the European Commission.

Chips JU

Chips JU was established in September, 2023, in an amendment to the Single Basic Act to implement the first pillar of the Chips Act and to continue the activities of its predecessors in the field of electronic components and systems (ECS). The Chips JU is a tri-partite partnership between the EC, the participating states and European industries; most of our actions are funded jointly and equally by these actors.

Chips Act: Entry into force, 21 September 2023

Signatures 13 September, Publication 18 September 2023

Roberta Metsola (European Parliament President)

José Manuel Albares Bueno (Council Presidency)

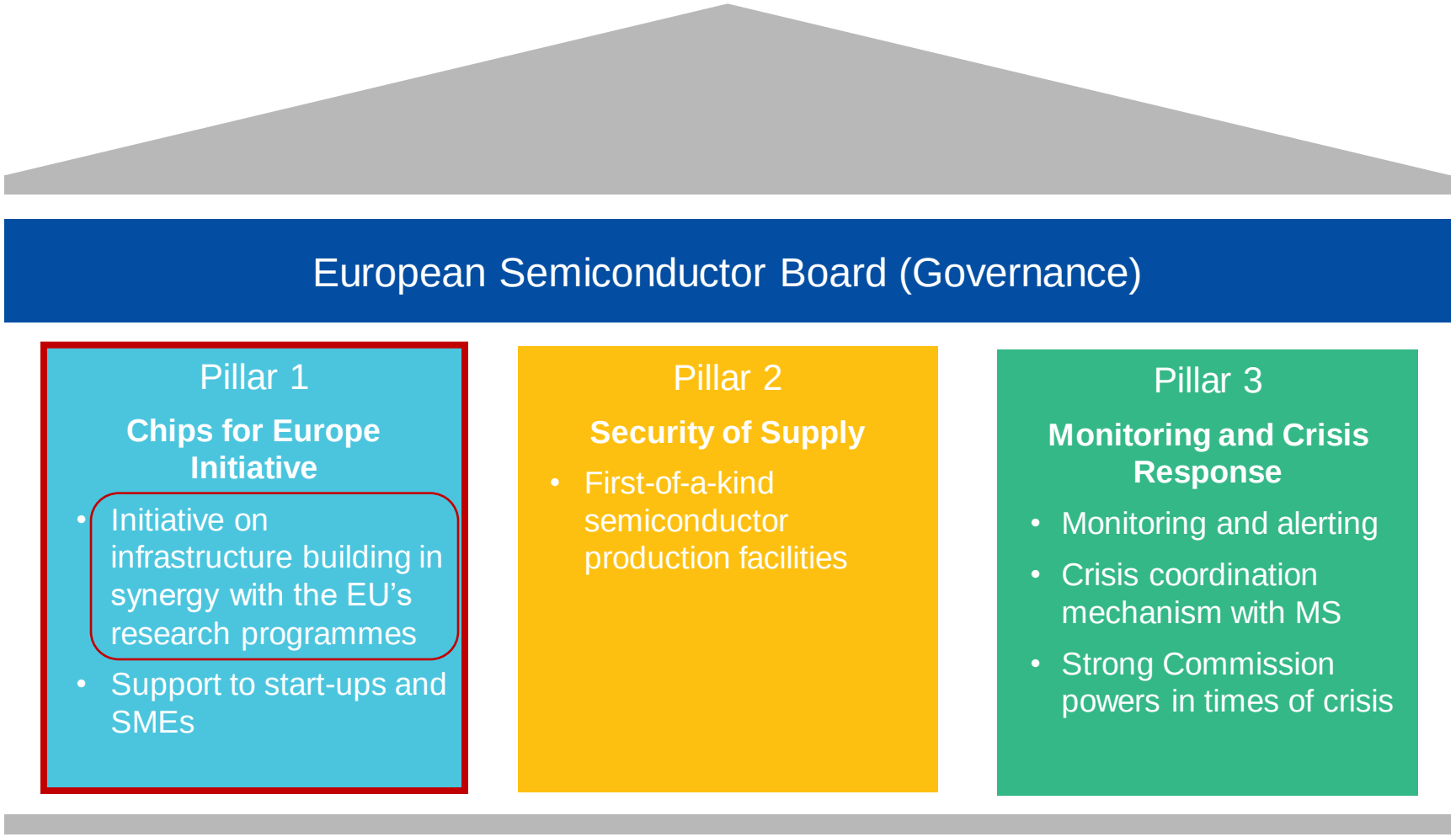
Chips Act:

https://eur-lex.europa.eu/eli/reg/2023/1781/oj

Single Basic Act amendment:

https://eur-lex.europa.eu/eli/reg/2023/1782/oj

THE 3 PILLARS OF THE CHIPS ACT



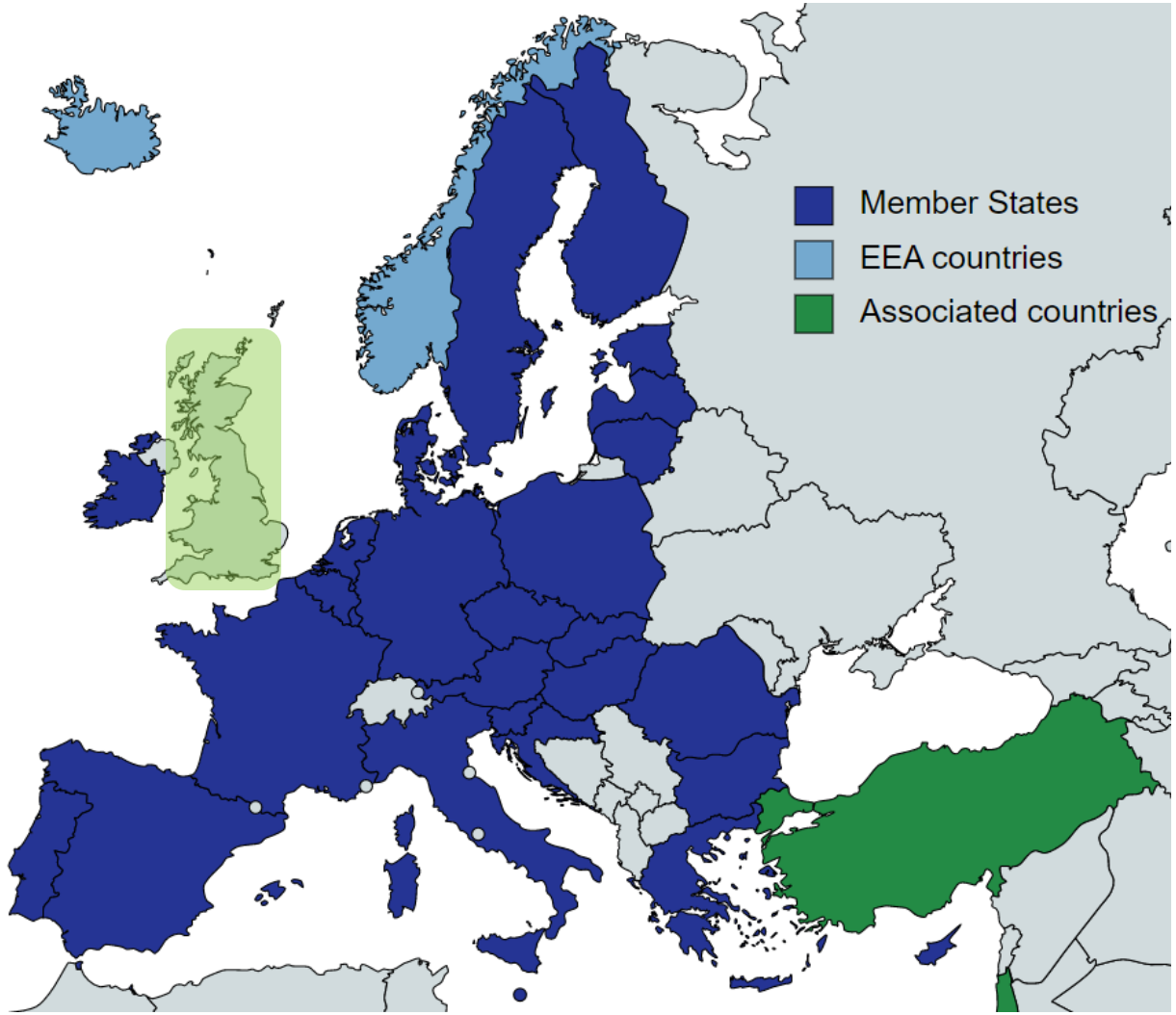
CHIPS JU AND ITS PREDECESSOR KEY DIGITAL TECHNOLOGIES JU (KDT JU)

Non-initiative

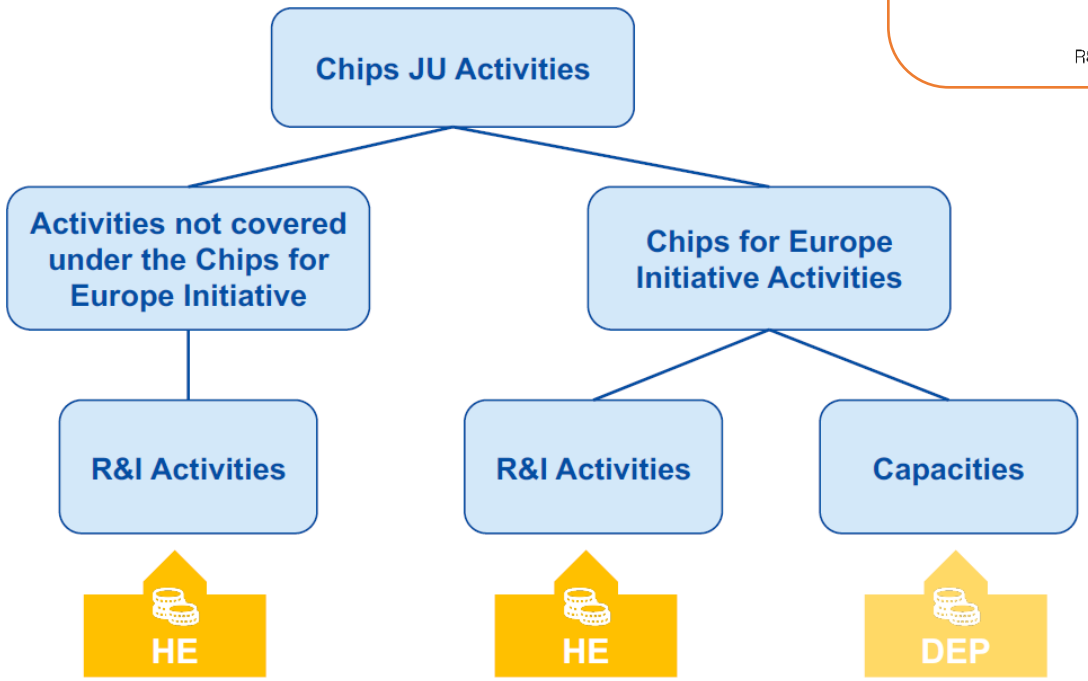
Initiative

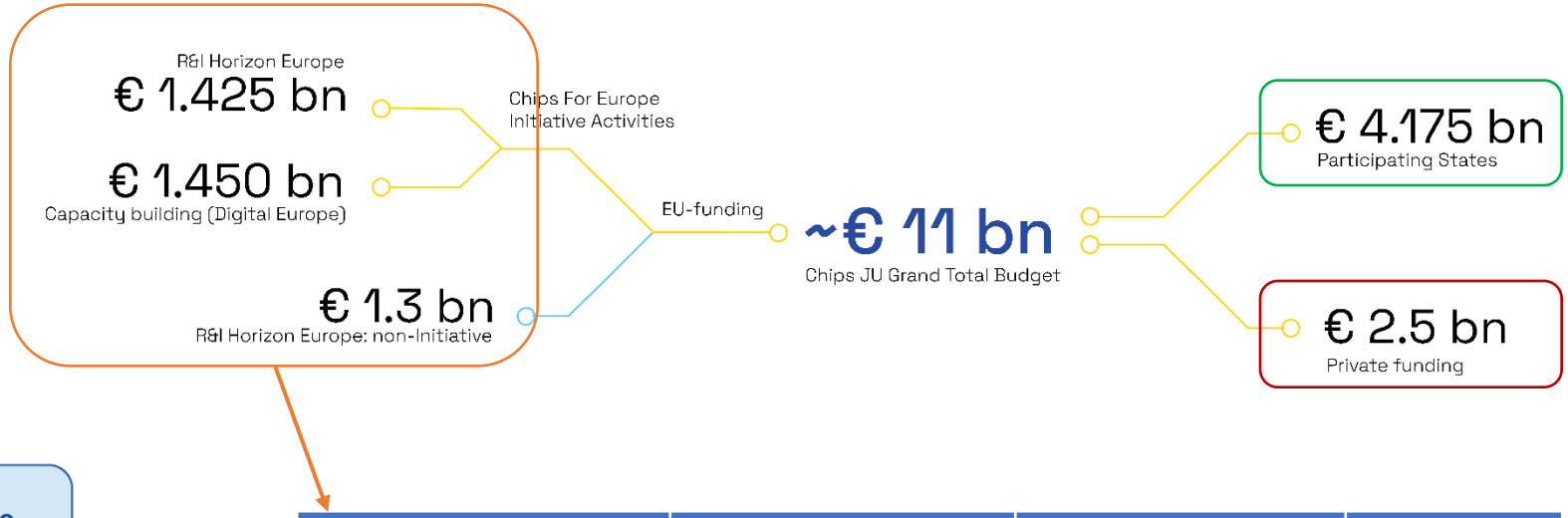
- **KDT General Objectives**
  - a) Reinforce EU strategic autonomy in electronic components and systems
  - b) Establish EU scientific excellence and innovation leadership
  - c) Ensure that components and systems technologies address Europe's societal and environmental challenges
- **From KDT to Chips JU**
  - d) Pilot lines
  - e) Design platform
  - f) Competence centers
  - g) Quantum chips technology

  Digital Europe Programme in addition to Horizon Europe
- **Disclaimed:** ***we know that the WP2023-2027 will need to be updated/amended in the spring and some details on the following pages may change:***
  https://www.chips-ju.europa.eu/Library/
- How to participate:
  https://www.chips-ju.europa.eu/Participate/



CHIPS JU





EU Contribution to Chips JU (excl	Chips for Europe Initiative	Non-Initiative	Total
R&I (Horizon Europe)	1.425	1.300	2.725
Cap building (DEP)	1.450	n.a.	1.450
Total	**2.875**	**1.300**	**4.175**

CHIPS JU NONE INITIATIVE CALLS 2024

Action	Title	Maximum JU Funding (M€)
HORIZON-Chips 2024-1-IA-T1	Global IA call according to SRIA 2024	**103.00**
HORIZON-Chips 2024-1-IA-T2	Focus topic on “High Performance RISC-V Automotive Processors supporting SDV”	**20.00**
HORIZON-Chips 2024-1-IA-T3	Focus topic on “Service Oriented Framework for the Software Defined Vehicle of the future"	**20.00**
HORIZON- Chips 2024-2-RIA-T1	Global RIA call according to SRIA 2023	**52.00**
HORIZON- Chips 2024-2-RIA-T2	Focus topic on “Sustainable and greener manufacturing”	**15.00**
HORIZON- Chips 2024-3-RIA	Joint call with Korea on Heterogeneous integration and neuromorphic computing technologies for future semiconductor components and systems	**6.00**
		216.00

Chips JU IA proposals

An IA proposal is characterized by:

- The activities have their centre of gravity at the **TRL 5-8.**
- Execution by **an industrial consortium** that may consist of large enterprises and SMEs but also including universities, institutes, public organizations
- Using **innovative technology**
- Establishment of a new and realistic innovation environment **connected with an industrial environment,** such as:
  - a pilot line facility capable of manufacturing
  - a zone of full-scale testing
  - a development of new processes or tools and their introduction in several domains
  - the development of frameworks or platforms together with the usage of these frameworks or platforms in innovative products.
- **Having a deployment plan** leading to short to **midterm economic value creation** in Europe.

Focus topic on High Performance RISC-V Automotive Processors Supporting SDV

- RISC-V still requires important extensions and add-ons in order to support *high-performance automotive quality processing* needs. To close this gap and facilitate the development of top-level automotive RISC-V processor cores, efforts should be focussed on the development of an **automotive RISC-V reference hardware platform, subject of this focus topic**.
- This **focus topic** concerns an **open-source RISC-V based hardware** system implementation of the **SDV Hardware Layer** compatible with one or multiple widely-agreed-upon **Hardware Abstraction Layers** of the vehicle of the future, **addressing the hardware development** part of an **overall system approach** for HW-SW co-design, more in particular **RISC-V based processor solutions** which are **optimized for SDV** implementations.
- The expected RISC-V reference platform shall be targeted for **commercial use** and should comply with **industry standards** with respect to quality and safety. It should contain all assets and collaterals needed to enable and accelerate the development and adoption of RISC-V cores throughout the European automotive ecosystem.

Focus topic on Software-define vehicle middleware and API framework for the vehicle of the future

- Europe needs to join forces in the automotive industrial domain by cooperating in an ecosystem-based technology initiative in order to lead on the Software Defined Vehicle technology and to capitalize on the expected gains on efficiency and development cost, complexity- reduction, and fulfilment of changing customer expectations.
- The SDV software stack (often also called Car OS) is extended by a **Middleware and Application Programming Interface (API) Framework** which supports different technologies. This framework abstracts the low-level technical details of the entire SDV SW stack towards the *SDV application layer*. It exposes the hardware functionalities directly as APIs or services also using a datacentric design in an OS independent, standardized & interoperable, safe, secure, efficient and easily accessible way.
- This call has a focus on the third layer, the *SDV Middleware and API Layer*.
  - ***Modular (open-source) building blocks and open architectures*** of the ***SDV middleware and API framework*** for the ***vehicle of the future***.
  - ***Holistic engineering framework***

Chips JU RIA proposals

A RIA proposal is characterized by:

- The activities have their centre of gravity at **TRL 3-4**.
- Execution by a consortium that may consist of SMEs, large enterprises, universities, institutes, public organizations;
- Developing **innovative technologies and/or using them in innovative ways**;
- Targeting **demonstration of the innovative approach** in a relevant product, service or capability, clearly addressing the applications relevant for societal challenges;
- Demonstrating **value and potential in a realistic lab environment** reproducing the targeted application;
- Having a **deployment plan showing the valorisation for the KDT ecosystem** and the contribution to the KDT goals and objectives.

Focus Topic Sustainable and Greener Manufacturing

- This focus topic concerns the development of a sustainable and greener semiconductor manufacturing through the reduction of its environmental footprint with a focus on materials. The results of the project are expected to contribute to the following outcomes:
  - Increase the use of environmentally friendly materials, chemicals and solvents.
  - Minimization of waste and emissions during production and processing
  - Prevention of a future scarcity of some critical materialsetals for SC processing through a more efficient and cost-effective products and electronic waste recycling in process., including chips and PCBs.

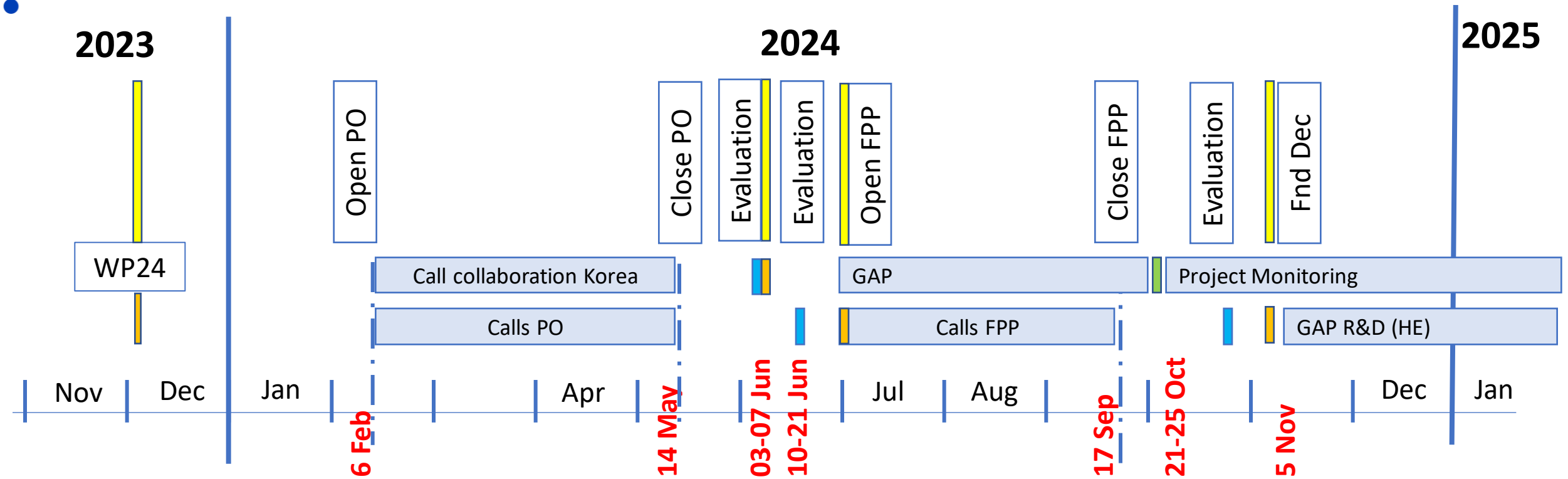
Joint call with Korea

- This joint call for proposals between the Republic of Korea and the EU dresses the topics related to Heterogeneous integration and neuromorphic computing technologies for future semiconductor components and systems and intends to set a framework
  - To strengthen the relation between R&I players in both jurisdictions
  - To undertake joint R&I for EU and Korean R&I teams by cooperating in pre-competitive projects on areas which are in the interest of both jurisdictions.
  - To build trust for further cooperation.
- This joint call topic will be co-funded by South Korea (KR) and the European Union (EU)
- This call has some very specific conditions. Please conslut the call text in the work programme

EU Funding Rates

Type of beneficiary	2024-1-IA	2024-1-IA Focus Topics	2024-2-RIA	2024-2-RIA Focus Topic	2024-3-IA
Large Enterprise	20 %	25 %	25 %	25 %	100%
SME	30 %	30 %	35 %	35 %	100%
University/Other (not for profit)	35 %	35 %	35 %	35 %	100%
National Funding	YES	YES	YES	YES	NO

Planning Calls 2024 Non-Initiative

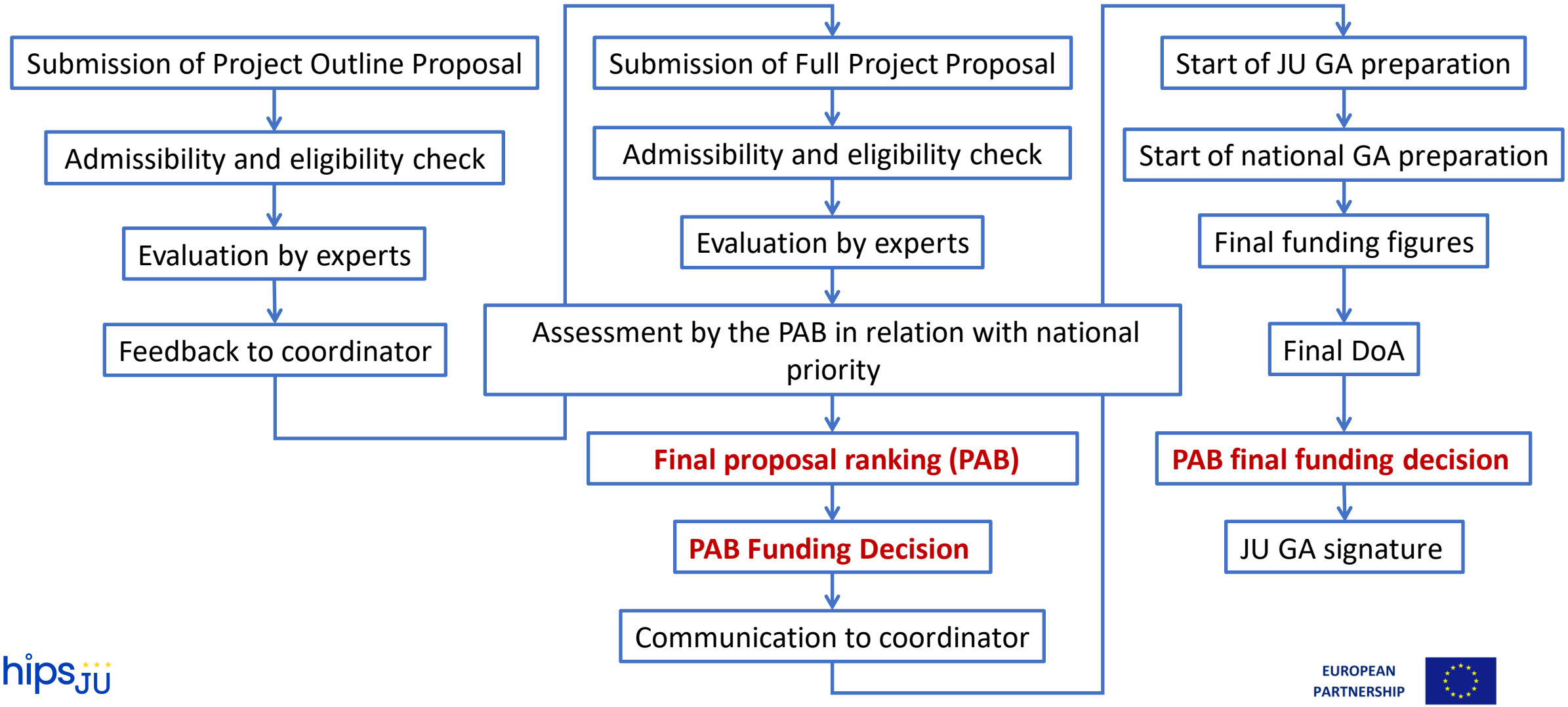


Schedule

Calls 2024-1 and 2024-2	Two stage Call with submission of Project Outline (PO) and Full Proposal (FPP)
Publication date	06 February 2024
Deadline PO Phase	14 May 2024 at 17:00 Brussels Time
Deadline FPP Phase	17 September 2024 at 17:00 Brussels Time
PAB selection	November 2024
Grant preparation	December 2024 to April 2025
Start of the projects	around May 2025

For the Call2024-3, there is no PO phase only an FPP phase with e deadline on 14 May 2024

Proposal Evaluation, Selection, and Grant Agreement Preparation



EUROPEAN PARTNERSHIP

Useful links

Check regularly the call information under the CHIPS website:

https://www.chips-ju.europa.eu/

Address eventual questions related to the calls to:

calls@chips-ju.europa.eu

Consult the sections on the 2024 calls in the:

Chips JU Work Programme